

ATW

AT8PU86LV

AT8PU86LV

Low Power Full-Speed USB Controller

Datasheet R02

October 20 2009

Version Control

Version	Date.	Description
R01	2009-06-01	Release of prototype
R02	2009-10-20	Modified GPIO Sink current

Contents

1.0 General Description.....	P.4
2.0 Feature.....	P.4
3.0 Block Diagram.....	P.4
4.0 Pin Definitions.....	P.5
5.0 Pin Description.....	P.5
6.0 Program Memory Mapping.....	P.6
7.0 Memory And Register Mapping.....	P.6
8.0 Instruction Set.....	P.20
9.0 Clock Control.....	P.22
9.1 Internal/External Oscillator Switch Operation.....	P.22
10.0 Reset.....	P.23
11.0 Suspend Mode.....	P.24
11.1 Detection of Resume.....	P.24
11.2 Remote Wake-up.....	P.24
12.0 General Purpose I/O Ports.....	P.24
13.0 PS2 mode.....	P.25
14.0 USB Transceiver.....	P.25
15.0 USB Serial Interface Engineer(SIE).....	P.25
15.1 Default Control Endpoint:EP0.....	P.25
15.2 Interrupt Transfer Endpoints:EP1 and EP2.....	P.25
15.3 Bulk Transfer Endpoints:EP3 and EP4.....	P.25
16.0 Micro-Controller.....	P.26
16.1 Timer0/1.....	P.26
16.2 Watchdog Timer(WDT).....	P.26
17.0 Capture Timer Register.....	P.26
18.0 Serial Peripheral Interface(SPI).....	P.27
18.1 Master Mode.....	P.27
18.1.1 Master Mode With SSE Control.....	P.27
18.1.2 Master Mode Without SSE Control.....	P.27
18.2 Slave Mode.....	P.28
18.2.1 Slave Mode with SSE Control.....	P.28
18.2.2 Slave Mode without SSE Control.....	P.28
19.0 SPI communication.....	P.29
20.0 Interrupt.....	P.29

21.0 Absolute Maximum Ratings.....	P.30
22.0 DC Characteristics.....	P.30
22.1 General.....	P.30
22.2 GPIO Interface.....	P.30
23.0 AC Characteristics.....	P.31
23.1 Clock Period.....	P.31
23.2 USB Timing.....	P.31
23.3 SPI Timing.....	P.31
24.0 Application Circuit.....	P.32
25.0 Package Diagrams.....	P.33

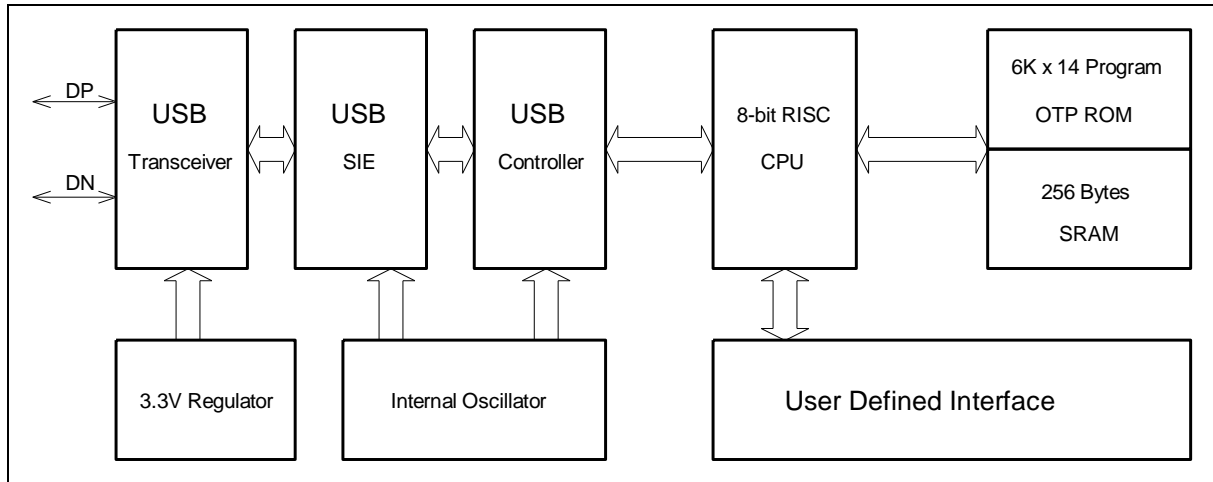
1.0 General Description

The AT8PU86LV is an 8-bit microprocessor embedded device tailored to the USB application. It includes an 8-bit RISC CPU core, 192~256 byte SRAM, Full Speed and Low Speed USB Interface and a 6K x 14 internal program OTP-ROM.

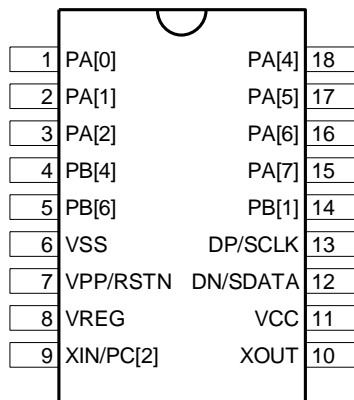
2.0 Features

- USB Specification Compliance
 - ◇ Support Full-Speed and Low-Speed USB 2.0 specification.
 - ◇ Built-in USB Transceiver.
 - ◇ Built-in 1.5k pull-high resistor.
 - ◇ Support one address and four 8-byte and two 32-byte data endpoints.
 - ◇ Support USB Suspend and Resume function.
 - ◇ One Control IN/OUT endpoints, two INT, BULK endpoints.
- 8-bit RISC microprocessor
 - ◇ 6K x 14 internal program OTP-ROM.
 - ◇ 256 bytes internal SRAM.
 - ◇ Optional 12MHz/24MHz internal MCU clock by configuration.
 - ◇ Optional Default/16MHz/12MHz/6MHz/58KHz internal MCU clock by firmware.
 - ◇ One Watch dog Timer, Timer0, Timer1, and two captures Timers.
- System Clock
 - ◇ Internal Clock Generator
 - 0.25% Accuracy after OTP calibration.
 - ◇ Internal slow oscillator 58KHz free run clock for suspend mode.
 - ◇ Built-in flexible programming PLL for external Oscillator or crystal
 - Operating Frequency Range of Oscillator/crystal is 2~48 MHz.
 - ◇ Optional external ceramic resonator or internal clock mode..
- 16-I/O ports
 - ◇ High current drive on any GPIO pin : 25mA/pin current sink.
 - ◇ Each GPIO pin supports high-impedance input, internal pull-ups, open drains output, or CMOS outputs.
- Power Manager and consumption
 - ◇ Power on reset (POR) is 2.0V
 - Chip can work on greater than 2.2V power.
 - ◇ Low Voltage Detect is 3.8V
 - ◇ Regulator 3.3V output, supply 45mA current.
 - ◇ MCU operating at 24MHz clock
 - Enable USB operating current is 17mA as Vcc=5V.
 - Disable USB operating current is 6mA as Vcc=3.3V.
 - ◇ MCU operating at 12MHz clock
 - Enable USB operating current is 13mA as Vcc=5V.
 - Disable USB operating current is 4mA as Vcc=3.3V
- **GPIO supply 1.8V~5V interface.**
- Support SSC to reduce EMI.

3.0 Block Diagram



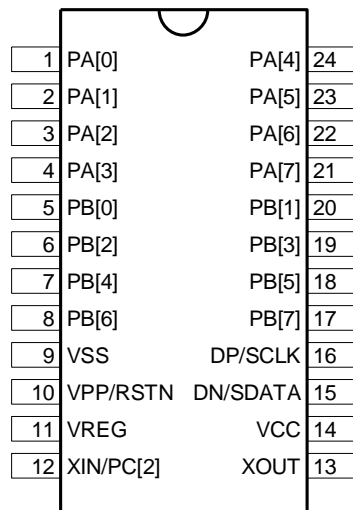
4.0 Pin Definitions



18-pin

AT8PU86A

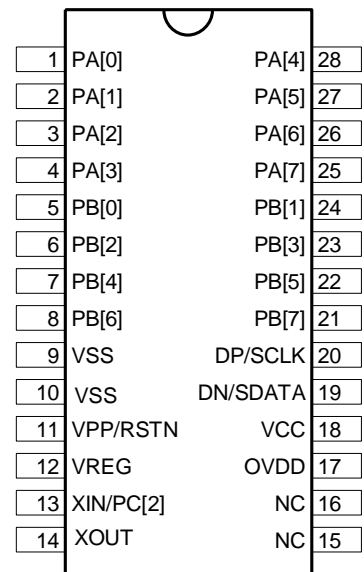
PDIP/SOP



24-pin

AT8PU86B

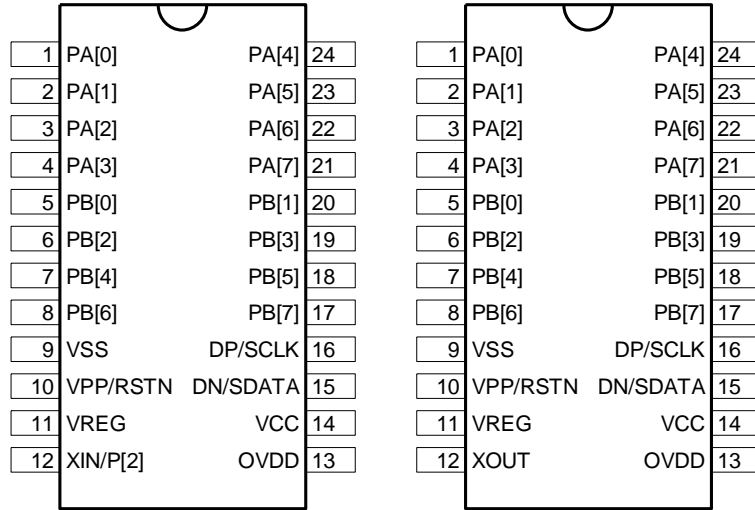
PDIP/SSOP/SOP



28-pin

AT8PU86I

PDIP/SSOP/SO



24-pin

AT8PU86C

PDIP/SSOP/SOP

24-pin

AT8PU86D

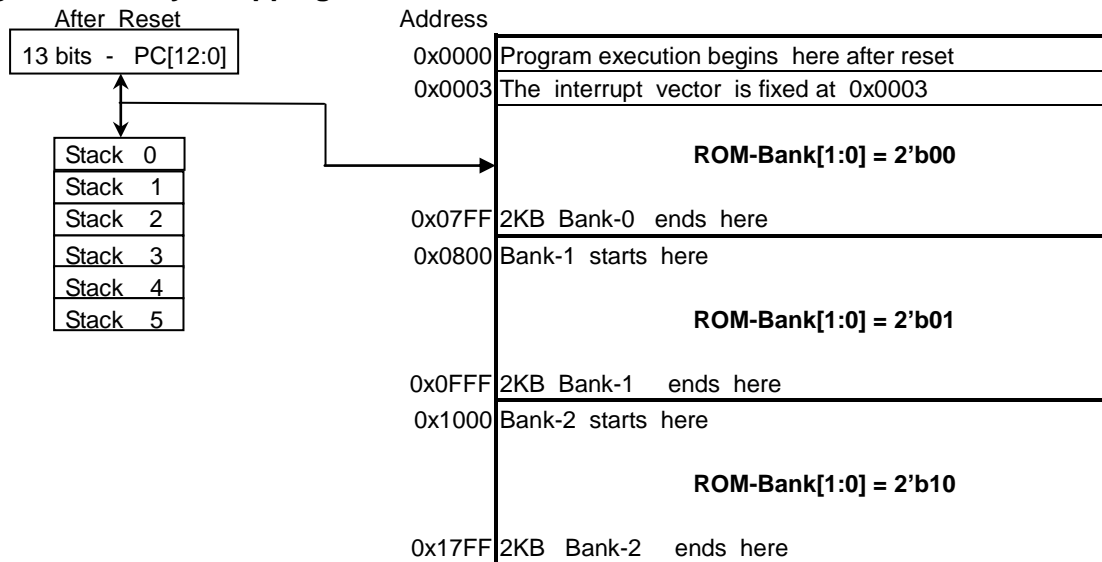
PDIP/SSOP/SOP

5.0 Pin Description

PIN Name	I/O	18-pin	24-pin	24-pin	24-pin	28-pin	Description	Note
		A	B	C	D	I		
PA[7:0]	IO	1,2,3,15,16,17,18,	1,2,34,21,22,23,24	1,2,34,21,22,23,24	1,2,34,21,22,23,24	1,2,3,4,25,26,27,28	GPIO Port A capable of sinking up to 25 mA/pin, or sinking controlled low or high programmable current. Can also source 2 mA current, provide a resistive pull-up, or serve as a high-impedance input. PA[0] and PA[1] provide inputs to Capture Timers A and B, respectively. Use PA[4]~PA[6] in SPI mode.	
PB[7:0]	IO	4,5,14	5,6,7,8,17,18,19,20	5,6,7,8,17,18,19,20	5,6,7,8,17,18,19,20	5,6,7,8,21,22,23,24	GPIO Port B capable of sinking up to 25 mA/pin, or sinking controlled low or high programmable current. Can also source 2 mA current, provide a resistive pull-up, or serve as a high-impedance input.	
VSS	G	6	9	9	9	9,10	Ground	
VPP	I	7	10	10	10	11	Programming voltage supply, VCC for normal operation	
RSTN	I						External reset pin , active low.	
VREG	O	8	11	11	11	12	3.3V Regulator output	
XIN PC[2]	I	9	12	12	--	13	2~48 MHz ceramic resonator or external clock input Port C [2]input	
XOUT	O	10	13	--	12	14	2~48 MHz ceramic resonator return pin; 24MHz(FS) or 6MHz(LS) internal oscillator output;	
NC	-	-	-	-	-	15,16	NC	
OVDD	P	-	-	13	13	17	I/O pad power Voltage supply 1.8 ~ 5 V	
VCC	P	11	14	14	14	18	Voltage supply(5V)	
DN SDATA	IO IO	12	15	15	15	19	USB differential data lines (D-) PS/2 data signal	

DP	IO	13	16	16	16	20	USB differential data lines (D+)	
SCLK	IO						PS/2 clock signal	

6.0 Program Memory Mapping



The AT8PU86LV has program memory size greater 2K works, but the CALL and GOTO instructions only have a 11-bits address range. This 11-bit address range allows a branch within a 2K program memory page size. To allow CALL and GOTO instructions to address the entire 6K program memory address range for FM8U86LV, there is another two bits to specify the program memory page. The paging bit comes from the ROMBANK[1:0] bits(PUMODE[6:5]). When doing a CALL or GOTO instruction, the user must ensure that page bit ROMBANK[1:0] are programmed so that the desired program memory page is addressed. When one of return instructions is executed, the entire 13-bit PC is POPed from the stack. Therefore, manipulation of the ROMBANK[1:0] is not required for return instructions.

7.0 Memory And Register Mapping

Table 7-1 I/O Register Mapping

RAMBNK[1:0] Address	Description			
	0 0 Bank 0	0 1 Bank 1	1 0 Bank 2	1 1 Bank 3
00h	INDF			
01h	TMR0			
02h	PCL			
03h	STATUS			
04h	FSR			
05h	PORTA			
06h	PORTB			
07h	PORTC			
08h	PCON			
09h	PBIE			
0Ah	PBCON			
0Bh	TMCON			
0Ch	INTEN			
0Dh	INTFLAG			
0Eh	INTEN1			

08h	PAMODE0
09h	PAMODE1
0Ah	PBMODE0
0Bh	PBMODE1
0Ch	PADRVM0
0Dh	PADRVM1
0Eh	PADRVM2

RAMBNK[1:0] Address	Description			
	0 0 Bank 0	0 1 Bank 1	1 0 Bank 2	1 1 Bank 3
0Fh	INTFLAG1			
10h	T0RLD			
11h	USBADDR			
12h	USBMDCFG			
13h	EP0RXST			
14h	EP0TXST			
15h	EP1TXST			
16h	EP2TXST			
17h	EP3TXST			
18h	EP4RXST			
19h	EPST1			
1Ah	TMR1			
1Bh	T1RLD			
1Ch	SPIRXB			
1Dh	SPITXB			
1Eh	SPISTAT			
1Fh	SPICON			
20H	PUMODE			
21H	CAPAR			
22H	CAPAF			
23H	CAPBR			
24H	CAPBF			
25H	CAPIE			
26H	CAPFLAG			
27H	CAPCON			
28H	CLKCFG			
29H	MPLL			
2AH	NPLL			
2Bh 2Fh	General Purpose Registers			
30h 3Fh	ENP0RX ENP0TX		ENP3TX0	ENP4RX0
40h 4Fh	ENP1TX ENP2TX		ENP3TX1	ENP4RX1
50h 7Fh	General Purpose Registers 0	General Purpose Registers 1	General Purpose Registers 2	General Purpose Registers 3

0Fh	PBDRVMD0
10h	PBDRVMD1
11h	PBDRVMD2

TABLE 7-2 : The Registers Controlled IOST or IOSTR Instructions

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
08h (w)	PAMODE0	Port A Mode Control Register							
09h (w)	PAMODE1								
0Ah (w)	PBMODE0	Port B Mode Control Register							
0Bh (w)	PBMODE1								
0Ch (w)	PADRVMD0	Port A Drive High Strength Mode Control Register							
0Dh (w)	PADRVMD1								
0Eh(w)	PADRVMD2								
0Fh (w)	PBDRVMD0	Port B Drive High Strength Mode Control Register							
10h(w)	PBDRVMD1								
11h (w)	PBDRVMD2								

Accessed by IOST/IOSTR instruction

The port I/O Control Registers are loaded with the contents of the ACC register by executing the IOST R (05h~06h) instruction. By executing the IOSTR instruction, user read these registers into ACC.

A '1' from a IOST register bit puts the corresponding output driver in hi-impedance state(input mode).

A '0' enables the output buffer and puts the contents of the output data latch on the selected pins (output).

The IOST registers are set all '1's(output drivers disabled) upon POWER RESET.

TABLE 7-2.1 Port A and B Output control truth Table

Data register	Mode1	Mode0	Output Drive Strength
1	0	0	HI-z(Input mode)
0			
1	0	1	Normal Drive
0			Sink (8mA)
1	1	0	Resistive(14KΩ)
0			Sink (2mA)
1	1	1	Normal Drive
0			Sink (25mA)

TABLE 7-2.2 PortA and B Output Drive Strength Truth Table

PADRVMD2	PADRVMD1	PADRVMD0	Output Drive Current
0	0	0	Default (Base on Table 7-2.1)
0	0	1	Drive high (1mA)
0	1	0	Normal Drive high (2mA)
0	1	1	Drive high (3mA)
1	0	0	Drive high (4mA)
1	0	1	Drive high (5mA)
1	1	0	Drive high (6mA)
1	1	1	Drive high (7mA)

TABLE 7-3: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
01h (r/w)	TMR0	8-bit real-time clock/counter							
02h (r/w)	PCL	Low order 8 bits of PC							

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
03h (r/w)	STATUS	--	--	--	/TO	/PD	Z	DC	C
04h (r/w)	FSR	--	Indirect data memory address pointer						
05h (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
06h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
07h (r)	PORTC	--	--	--	--	--	--	IOC1	IOC0
08h (r/w)	PCON	WDTE	WDTSL	WDTPS2	WDTPS1	WDTPS0	PORE	PDCLK	--
09h (r/w)	PBIE	PBIE7	PBIE6	PBIE5	PBIE4	PBIE3	PBIE2	PBIE1	PBIE0
0Ah (r/w)	PBCON	PBCON7	PBCON6	PBCON5	PBCON4	PBCON3	PBCON2	PBCON1	PBCON0
0BH(r/w)	TMCON	T1ON	T1PS2	T1PS1	T1PS0	T0ON	T0PS2	T0PS1	T0PS0
0Ch (r/w)	INTEN	GIE	--	--	RSTIE	SPITXIE	SPIRXIE	T1IE	T0IE
0Dh (r/w)	INTFLAG	PBIF	--	--	RSTIF	SPITXIF	SPIRXIF	T1IF	T0IF
0Eh (r/w)	INTEN1	RSMIE	SUSIE	RX0IE	TX0IE	TX1IE	TX2IE	TX3IE	RX4IE
0Fh (r/w)	INTFLAG1	RSMIF	SUSIF	RX0IF	TX0IF	TX1IF	TX2IF	TX3IF	RX4IF
10h (r/w)	TORLD	TORD7	TORD6	TORD5	TORD4	TORD3	TORD2	TORD1	TORD0
11h(r/w)	USBADDR	EUSBAR	USBAR6	USBAR5	USBAR4	USBAR3	USBAR2	USBAR1	USBAR0
12h(r/w)	USBMDCFG	SUSPMD	RESMD	CTRRD	RX0RDY	EP1CFG	EP2CFG	EP3CFG	EP4CFG
13h(r)	EP0RXST	RX0TGL	RX0ERR	EP0DIR	EP0SET	RX0CN3	RX0CN2	RX0CN1	RX0CN0
14h(r/w)	EP0TXST	TX0RDY	TX0TGL	EP0STAL	--	TX0CN3	TX0CN2	TX0CN1	TX0CN0
15h(r/w)	EP1TXST	TX1RDY	TX1TGL	EP1STAL	--	TX1CN3	TX1CN2	TX1CN1	TX1CN0
16h(r/w)	EP2TXST	TX2RDY	TX2TGL	EP2STAL	--	TX2CN3	TX2CN2	TX2CN1	TX2CN0
17h(r/w)	EP3TXST	TX3RDY	TX3TGL	TX3CN5	TX3CN4	TX3CN3	TX3CN2	TX3CN1	TX3CN0
18h(r)	EP4RXST	RX4TGL	RX4ERR	RX4CN5	RX4CN4	RX4CN3	RX4CN2	RX4CN1	RX4CN0
19h(r/w)	EPST1	RX4RDY	EP4STAL	EP3STAL	LVDI	LVR	CLKSW	SELCLK1	SELCLK0
1Ah(r/w)	TMR1	TM17	TM16	TM15	TM14	TM13	TM12	TM11	TM10
1Bh(r/w)	T1RLD	T1RD7	T1RD6	T1RD5	T1RD4	T1RD3	T1RD2	T1RD1	T1RD0
1Ch(r)	SPIRXB	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0
1Dh(r)	SPITXB	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0
1Eh(r/w)	SPISTAT	--	--	TXBF	TM1IF	SDOOD	SCKOD	--	RXBF
1FH(r/w)	SPICON	CKEDG	SPION	RXOV	SSE	SSEMOD	SPIM2	SPIM1	SPIM0
20h(r/w)	PUMODE	USBMD	ROMBNK1	ROMBNK0	--	RAMBNK1	RAMBNK0	PS2EN	USBEN
21h(r)	CAPAR	Capture_A rising Data register							
22h(r)	CAPAF	Capture_A Falling Data register							
23h(r)	CAPBR	Capture_B rising Data register							
24h(r)	CAPBF	Capture_B Falling Data register							
25h(r/w)	CAPIE	--	--	--	--	CAPBFIE	CAPBRIE	CAPAFIE	CAPARIE
26h(r/w)	CAPFLAG	--	--	--	--	CAPBFIF	CAPBRIF	CAPAFIF	CAPARIF
27h(r/w)	CAPCON	--	--	CAPBON	CAPAON	FEH	CAPPS2	CAPPS1	CAPPS0
28h(r/w)	CLKCFG	XTBUF3	XTBUF2	XTBUF1	XTBUF0	INSDY	INCODS	EXOSEN	IRCEN
29h(r/w)	MPLL	MPLL7	MPLL6	MPLL5	MPLL4	MPLL3	MPLL2	MPLL1	MPLL0
2Ah(r/w)	NPLL	NPLL7	NPLL6	NPLL5	NPLL4	NPLL3	NPLL2	NPLL1	NPLL0

Legend: - = unimplemented, read as '0',

Address 00H : Indirect Addressing Register (INDF)

Bits	Description	Read	Write	Default
7~0	Uses contents of FSR to address data memory	Yes	Yes	00h

Address 01H : Timer0(TMR0)

Bits	Description	Read	Write	Default
7~0	Timer 0	Yes	Yes	00h

Address 02H: Low bytes of Program Counter(PCL)

Bits	Description	Read	Write	Default
7~0	Low bytes of Program Counter(7~0)	Yes	Yes	00h

Address 03H : Status Register(STATUS)

Bits	Name	Description	Read	Write	Default
7~5	Revered	Revered	No	No	0
4	/TO	WDT overflow flag bit (0: active)	Yes	No	1
3	/PD	Power down flag bit (0: active)	Yes	No	1
2	Z	Zero flag	Yes	Yes	0
1	DC	Decimal carry flag or decimal/borrow flag	Yes	Yes	0
0	C	Carry flag or/borrow flag	Yes	Yes	0

Address 04H :File select Register(FSR)

Bits	Name	Description	Read	Write	Default
7	Revered	Revered	No	No	0
6~0	FSR	File select register to define address in indirect addressing mode	Yes	Yes	0

Address 05H : Port A (PORTA)

Bits	Name	Description	Read	Write	Default
7~0	PORTA	Port A data input/output	Yes	Yes	00h

Address 07H :Port C (PORTC)

Bits	Name	Description	Read	Write	Default
7~3	Reversed	Revered	Yes	No	00h
2	PORTC[2]	In the internal clock mode. The XIN pin can serve as a general purpose input.	Yes	No	X
1	PORTC[1]	D+(SCLK).The state of the D+ pins can be read at Port C data register.	Yes	Yes	1
0	PORTC[0]	D-(SDATA).The state of the D- pins can be read at Port C data register.	Yes	Yes	1

Address 08H : Power Control Register (PCON)

Bits	Name	Description	Read	Write	Default
7	WDTE	Watch-dog timer enable (0:disable,1:enable)	Yes	Yes	1
6	WDTSL	Watch-dog timer out select . 1: If Watch-dog timer out ,the Device be reset. PC=0000h; 0: If Watch-dog timer out ,Device only SUSPMD(12.7H) be clear by H/w. PC= PC + 1;	Yes	Yes	1
5~3	WDTPS[2:0]	WDT prescaler	Yes	Yes	0h
2	PORE	Power on reset detector 1: enable 0:disable	Yes	Yes	1h
1	PDCLK	SIE clock enable , 1: SIE clock disable 0: SIE clock enable	Yes	Yes	0h
0	Revered	Revered	Yes	No	0h

WDTPS[2:0]	WDT time out
3'b000	18ms*1 = 18ms
3'b001	18ms*2 = 36ms

3'b010	18ms*4 = 72ms
3'b011	18ms*8 = 144ms
3'b100	18ms*16 = 288ms
3'b101	18ms*32 = 572ms
3'b110	18ms*64 = 1152ms
3'b111	18ms*128 = 2304ms

TABLE 7-4 WDT Prescaler

Address 09H : Port B Interrupt Control Register (PBIE)

Bits	Name	Description	Read	Write	Default
7~0	PBIE	Port B or Port A interrupt enable bits (0:disable , 1:enable)	Yes	Yes	00h

Note : The XTBUF[3] of CLKCFG(28h) register bit (1 : select port B(default) , 0: select port A)

Address 0AH : Port B Wake-up Control Register (PBCON)

Bits	Name	Description	Read	Write	Default
7~0	PBCON	0 : falling edge(port B or port A), 1: Pin-changed (port B or port A)	Yes	Yes	00h

Address 0BH : Timer control Register(TMCON)

Bits	Name	Description	Read	Write	Default
7	T1ON	Timer1 module Enable bit	Yes	Yes	0
6~4	T1PS2~0	Timer1 Prescaler Rate 0:1/2 , 1:1/4 , 2:1/8 , 3:1/16,4:1/32,5:1/64,1:1/128,7:1/256	Yes	Yes	0h
3	T0ON	Timer0 module Enable bit	Yes	Yes	0
2~0	T0PS2~0	Timer0 Prescaler Rate 0:1/2 , 1:1/4 , 2:1/8 , 3:1/16,4:1/32,5:1/64,6:1/128,7:1/256	Yes	Yes	0h

T0/1 SP2,SP1,SP0	Prescaler Rate	Number of MCU clock
3'b000	1/2	4
3'b001	1/4	8
3'b010	1/8	16
3'b011	1/16	32
3'b100	1/32	64
3'b101	1/64	128
3'b110	1/128	256
3'b111	1/256	512

TABLE 7-5 Timer0/1 Prescaler

Address 0CH : Interrupt Mask Register(INTEN)

Bits	Name	Description	Read	Write	Default
7	GIE	Global Interrupt enable bit (0:disable,1:enable)	Yes	Yes	0
6	Revered	Revered	Yes	No	0
5	SOFIE	SOF interrupt enable bit.	Yes	Yes	0
4	RSTIE	USB bus reset interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
3	SPITXIE	SPI Transmit Interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
2	SPIRXIE	SPI Receive Interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
1	T1IE	Timer1 Interrupt enable bit. (0:disable,1:enable).	Yes	Yes	0
0	T0IE	Timer0 Interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0

Address 0DH : Interrupt Flag Register(INTFLAG)

Bits	Name	Description	Read	Write	Default
------	------	-------------	------	-------	---------

7	PBIF	Port B interrupt flag, write 0 clear flag	Yes	Yes	0
6	Revered	Revered	Yes	No	0
5	SOFIF	SOF packet is received flag, write 0 clear flag.	Yes	Yes	0
4	RSTIF	USB bus reset interrupt flag, write 0 clear flag	Yes	Yes	0
3	SPITXIF	SPI Transmit Interrupt flag ,write 0 clear flag	Yes	Yes	0
2	SPIRXIF	SPI Receive Interrupt flag, write 0 clear flag	Yes	Yes	0
1	T1IF	Timer1 Interrupt flag, write 0 clear flag	Yes	Yes	0
0	T0IF	Timer0 Interrupt flag, write 0 clear flag	Yes	Yes	0

Address 0EH : Interrupt Mask Register1(INTEN1)

Bits	Name	Description	Read	Write	Default
7	RSMIE	USB resume interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
6	SUSIE	USB suspend interrupt enable bit .(0:disable,1:enable)	Yes	Yes	0
5	RX0IE	Endpoint 0 received successfully interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
4	TX0IE	Endpoint 0 transmit successfully interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
3	TX1IE	Endpoint 1 transmit successfully interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
2	TX2IE	Endpoint 2 transmit successfully interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
1	TX3IE	Endpoint 3 transmit successfully interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0
0	RX4IE	Endpoint 4 received successfully interrupt enable bit. (0:disable,1:enable)	Yes	Yes	0

Address 0FH : Interrupt Flag Register1(INTFLAG1)

Bits	Name	Description	Read	Write	Default
7	RSMIF	USB resume interrupt flag, write 0 clear flag	Yes	Yes	0
6	SUSIF	USB suspend interrupt flag, write 0 clear flag	Yes	Yes	0
5	RX0IF	Endpoint 0 received successfully interrupt flag, write 0 clear flag	Yes	Yes	0
4	TX0IF	Endpoint 0 transmit successfully interrupt flag, write 0 clear flag	Yes	Yes	0
3	TX1IF	Endpoint 1 transmit successfully interrupt flag, write 0 clear flag	Yes	Yes	0
2	TX2IF	Endpoint 2 transmit successfully interrupt flag, write 0 clear flag	Yes	Yes	0
1	TX3IF	Endpoint 3 transmit successfully interrupt flag, write 0 clear flag	Yes	Yes	0
0	RX4IF	Endpoint 4 received successfully interrupt flag, write 0 clear flag	Yes	Yes	0

Note : The Endpoint 1,2,3,4 (ACK,NAK) interrupts are base on XTBBUF[0] (28H Register)

Address 10H: Timer0 overflow reload value(TORLD)

Bits	Name	Description	Read	Write	Default
7~0	TORLD	Timer0 overflow reload value	Yes	Yes	00h

Address 11H : USB address(USBADDR)

Bits	Name	Description	Read	Write	Default
7	EUSBAR	Device Address Enable 1: Enable Device Address 0: Disable Device Address	Yes	Yes	0
6~0	USBAR	USB device address	Yes	Yes	00h

Address 12H: USB Mode and Endpoint configuration (USBMDCFG)

Bits	Name	Description	Read	Write	Default
7	SUSPMD	F/W force USB interface to go into suspend mode	Yes	Yes	0
6	RESMD	F/W force USB interface send Resume signal in suspend mode	Yes	Yes	0
5	CTRRD	H/W will stall an invalid OUT token during control read transfer	Yes	Yes	0
4	RX0RDY	Endpoint 0 ready for receive, clear by H/ W RX0IF occurs	Yes	Yes	0
3	EP1CFG	Set endpoint 1 configuration	Yes	Yes	0
2	EP2CFG	Set endpoint 2 configuration	Yes	Yes	0

1	EP3CFG	Set endpoint 3 configuration	Yes	Yes	0
0	EP4CFG	Set endpoint 4 configuration	Yes	Yes	0

Address 13H: Endpoint 0 received status (EP0RXST)

Bits	Name	Description	Read	Write	Default
7	RX0TGL	1:Received DATA1(PID) packet ; 0 : Received DATA0 PID Packet	Yes	No	X
6	RX0ERR	EP0 received data error	Yes	No	X
5	EP0DIR	1: IN transfer 0:OUT/SETUP transfer	Yes	No	X
4	EP0SET	SETUP token indicator	Yes	No	X
3~0	RX0CNT	EP0 received data byte count	Yes	No	0h

Address 14H: Endpoint 0 transmit status (EP0TXST)

Bits	Name	Description	Read	Write	Default
7	TX0RDY	EP0 ready for transmit ,clear by H/W while TX0IF occurs	Yes	Yes	0
6	TX0TGL	EP0 transmit DATA1/DATA0 PID packet	Yes	Yes	0
5	EP0STAL	EP0 will stall OUT/IN packet while this bit set 1	Yes	Yes	0
4	Revered	Revered	Yes	No	0
3~0	TX0CNT	EP0 transmit data byte count	Yes	Yes	0h

Address 15H: Endpoint 1 transmit status (EP1TXST)

Bits	Name	Description	Read	Write	Default
7	TX1RDY	EP1 ready for transmit ,clear by H/W while TX1IFoccurs	Yes	Yes	0
6	TX1TGL	EP1 transmit DATA1/DATA0 PID packet	Yes	Yes	0
5	EP1STAL	EP1 will stall IN packet while this bit set 1	Yes	Yes	0
4	Revered	Revered	Yes	No	0
3~0	TX1CNT	EP1 transmit data byte count	Yes	Yes	0h

Address 16H: Endpoint 2 transmit status (EP2TXST)

Bits	Name	Description	Read	Write	Default
7	TX2RDY	EP2 ready for transmit ,clear by H/W while TX2IF occurs	Yes	Yes	0
6	TX2TGL	EP2 transmit DATA1/DATA0 PID packet	Yes	Yes	0
5	EP2STAL	EP2 will stall IN packet while this bit set 1	Yes	Yes	0
4	Revered	Revered	Yes	No	0
3~0	TX2CNT	EP2 transmit data byte count	Yes	Yes	0h

Address 17H: Endpoint 3 transmit status (EP3TXST)

Bits	Name	Description	Read	Write	Default
7	TX3RDY	EP3 ready for transmit ,clear by H/W while TX3IF occurs	Yes	Yes	0
6	TX3TGL	EP3 transmit DATA1/DATA0 PID packet	Yes	Yes	0
5~0	TX3CN	EP3 transmit data byte count	Yes	Yes	00h

Address 18H: Endpoint 4 received status (EP4RXST)

Bits	Name	Description	Read	Write	Default
7	RX4TGL	1:Received DATA1(PID) packet ; 0 : Received DATA0 PID Packet;	Yes	No	X
6	RX4ERR	EP4 received data error	Yes	No	X
5~0	RX4CNT	EP4 received data byte count	Yes	No	00h

Address 19H : Endpoint status register 1(EPST1)

Bits	Name	Description	Read	Write	Default
------	------	-------------	------	-------	---------

7	RX4RDY	EP4 ready for receive, clear by H/W while RX4IF occurs	Yes	Yes	0
6	EP4STAL	EP4 will stall OUT packet while this bit set 1	Yes	Yes	0
5	EP3STAL	EP3 will stall IN packet while this bit set 1	Yes	Yes	0
4	LVDT	0 : VBUS voltage less than 3.8 V 1 : VBUS voltage greater than 3.8V	Yes	No	X
3	LVR	0: When LVDT is high or low, Device still normal work. 1: When LVDT is low , Device will be cleared SUSPEN(12.7H) bit by H/W.	Yes	Yes	0h
2	CLKSW	0 : Don't switch clock . 1: Start to switch from default clock to select clock	Yes	Yes	0h
1:0	SELCLK[1:0]	2'b00 : Select MCU clock is 16MHz 2'b01 : Select MCU clock is 12MHz 2'b10 : Select MCU clock is 6MHz 2'b 11 : Select MCU clock is 58KHz	Yes	Yes	00h

CLKSW	SELCLK[1:0]	MCU Clock
0	2'bXX	6MHz or 12MHz or 24 MHz (base on clock of configuration)
0->1	2'b00	Switch MCU clock is from default clock to 16MHz clock
0->1	2'b01	Switch MCU clock is from default clock to 12MHz
0->1	2'b10	Switch MCU clock is from default clock to 6MHz
0->1	2'b11	Switch MCU clock is from default clock to 58KHz

TABLE 7-5 MCU clock select table

Address 1AH : Timer1(TMR1)

Bits	Name	Description	Read	Write	Default
7~0	TM1	8-bit counter	Yes	Yes	00h

Address 1BH: Timer1 overflow reload value(T1RLD)

Bits	Name	Description	Read	Write	Default
7~0	T1RLD	Timer1 overflow reload value	Yes	Yes	00h

Address 1CH: SPI Receive Buffer Register (SPIRXB)

Bits	Name	Description	Read	Write	Default
7~0	RX	Once the 8-bits data have been received, the data in SPI shift register (SPISR) will be moved to the SPIRXB register. The data must be read out before the next 8-bits data reception is completed if needed. The RXBF flag is set when the data in SPISR is moved to the SPIRXB register, and cleared as the SPIRXB register reads.	Yes	Yes	XXh

Address 1DH: SPI transmit Buffer Register (SPITXB)

Bits	Name	Description	Read	Write	Default
7~0	TX	Once the first valid clock pulse appear on SCK pin, the data in SPITXB will be loaded into SPISR and start to shift in/out. The new data must be written to SPITXB before the 8-bits data transmission is completed if needed. The TXBF flag is set when the data in SPITXB is moved to the SPISR register, and cleared as the SPITXB register writes.	Yes	Yes	XXh

Address 1EH: SPI Status Register (SPISTAT)

Bits	Name	Description	Read	Write	Default
7~6	Revered	Revered	Yes	No	0
5	TXBF	SPI transmit buffer empty flag.	Yes	Yes	0

4	TM1IF	SPI receive complete interrupt flag in Timer 1 mode. Set when receiving complete, reset by software.	Yes	Yes	0
3	SDOOD	1:Open-drain 0: Normal-drive control bit for SDO pin output	Yes	Yes	0
2	SCKOD	1: Open-drain 0: Normal-drive control bit for SCK pin output	Yes	Yes	0
1	Revered	Revered	Yes	No	0
0	RXBF	SPI receive buffer full flag. Set when the data in SPISR is moved to the SPIRXB register, reset by software or reading SPIRXB register	Yes	Yes	0

Address 1FH: SPI Control Register (SPICON)

Bits	Name	Description	Read	Write	Default
7	CKEDG	Clock edge select bit	Yes	Yes	0
6	SPION	SPI module enable bit. (0:disable,1:enable)	Yes	Yes	0
5	RXOV	SPI receive buffer overflow bit (only in slave mode)	Yes	Yes	0
4	SSE	SPI shift register enable bit.(0:disable,1:enable) 0:Reset by hardware as soon as the shifting is complete 1:Start to transmit/receive, and keep on "1" while the current byte is still begin transmitted/received. Note: When SSEMOD is set, the SSE is a "don't care".	Yes	Yes	0
3	SSEMOD	SSE bit control enable bit.(0:disable,1:enable) 0:Enable the SSE bit control. It means the SCK input/output will be inhibited of SSE=0 1:Disable the SSE bit control. It means the SCK input/output direct.	Yes	Yes	0
2~0	SPIM	SPI mode setting	Yes	Yes	0

SPIM[2:0]	SSP MODE
3'b000	SPI master mode, clock(SCK) = $F_{cpuclk} / 2$
3'b001	SPI master mode, clock (SCK)= $F_{cpuclk} / 4$
3'b010	SPI master mode, clock(SCK) = $F_{cpuclk} / 8$
3'b011	SPI master mode, clock(SCK) = $F_{cpuclk} / 16$
3'b100	SPI master mode, clock(SCK) = $F_{cpuclk} / 32$
3'b101	SPI slave mode, clock =SCK pin, SSB pin control enabled
3'b110	SPI slave mode, clock =SCK pin, SSB pin control disabled
3'b111	SPI master mode, clock(SCK) = (Timer1 output)/2

TABLE 7-5 SPI Mode

Address 20H: PS2/USB Detect Mode (PUMODE)

Bits	Name	Description	Read	Write	Default
7	USBMD	USB mode select. 1 : Full_Speed mode 0:Low_speed mode	Yes	Yes	1
6~5	ROMBNK[1:0]	ROM bank select bits 2'b00 : Bank-0 ; 2'b01:Bank-1;2'b10:Bank-2;2'b11:Reversed	Yes	Yes	0h
4	Revered	Revered	Yes	No	0
3~2	RAMBNK[1:0]	RAM bank select bits 2'b00 : Bank-0 ; 2'b01:Bank-1;2'b10:Bank-2;2'b11:Bank-3	Yes	Yes	0h
1	PS2EN	Enable PS2 D+ ,D- pull-up 4.7k Ω resistors	Yes	Yes	0
0	USBEN	Enable USB D+ or D- pull-up 1.5K Ω resistor	Yes	Yes	0

{ PS2EN , USBEN } = 2'b 00: Detect Mode ; 2'b01: Set USB Mode ; 2'b10: Set PS2 Mode ; 2'b11: USB Test

1. After Power-on reset, The PUMODE[1:0] default value is 2'b 00. The device have 200K Ω pull-up resistors on D+/D- line.
2. If D+/CLK(portc[1]), D-/Data(portc[0]) status are 2'b00, microprocessor set PUMODE[0] = 1. Otherwise

microprocessor set PUMODE[1] = 1.

3. When Device is defined USB mode , the D- or D+ line will be enable 1.5KΩ Pull-up resistor to 3.3V ,and disable 200KΩ pull-up Resistor.
4. When Device is defined PS/2 mode , the D- and D+ will be enable 4.7KΩ pull-up resistor to Vcc(5V).

Address 21H: Capture_A rising register (CAPAR)

Bits	Name	Description	Read	Write	Default
7~0	CAPAR	Capture Timer A -rising data for GPIO PA[0]	Yes	No	00

Address 22H: Capture_A Falling register (CAPAF)

Bits	Name	Description	Read	Write	Default
7~0	CAPAF	Capture Timer A-Falling Data for GPIO PA[0]	Yes	No	00

Address 23H: Capture_B rising register (CAPBR)

Bits	Name	Description	Read	Write	Default
7~0	CAPBR	Capture Timer B-Rising Data for GPIO PA[1]	Yes	No	00

Address 24H: Capture_B Falling register (CAPBF)

Bits	Name	Description	Read	Write	Default
7~0	CAPBF	Capture Timer B-Falling Data for GPIO PA[1]	Yes	No	00

Address 25H: Capture Status register (CAPIE)

Bits	Name	Description	Read	Write	Default
7~4	Revered	-	Yes	No	0
3	CAPBFIE	Capture B Falling Interrupt Enable bit(0:disable,1:enable)	Yes	Yes	0
2	CAPBRIE	Capture B Rising Interrupt Enable bit (0:disable,1:enable)	Yes	Yes	0
1	CAPAFIE	Capture A Falling Interrupt Enable bit(0:disable,1:enable)	Yes	Yes	0
0	CAPARIE	Capture A Rising Interrupt Enable bit(0:disable,1:enable)	Yes	Yes	0

Address 26H: Capture Status register (CAPFLAG)

Bits	Name	Description	Read	Write	Default
7~4	Revered	-	Yes	No	0
3	CAPBFIF	Capture B Falling Interrupt write 0 clear flag	Yes	Yes	0
2	CAPBRIF	Capture B Rising Interrupt write 0 clear flag	Yes	Yes	0
1	CAPAFIF	Capture A Falling Interrupt write 0 clear flag	Yes	Yes	0
0	CAPARIF	Capture A Rising Interrupt write 0 clear flag	Yes	Yes	0

Address 27H: Capture Control register (CAPCON)

Bits	Name	Description	Read	Write	Default
7~6	Revered	Revered	Yes	No	0
5	CAPBON	Capture B counter enable bit. (1: start , 0 : clear)	Yes	Yes	0
4	CAPAON	Capture A counter enable bit. (1: start , 0 : clear)	Yes	Yes	0
3	FEH	First Edge Hold	Yes	Yes	0
2~0	CAPPS[2:0]	Prescale bits	Yes	Yes	0

Bit 3: First Edge Hold

1 = The time of the first occurrence of an edge is held in the Capture Timer Data Register until the data is read.

Subsequent edges are ignored until the Capture Timer Data Register is read.

0 = The time of the most recent edge is held in the Capture Timer Data Register. That is, if multiple edges have occurred before reading the capture timer, the time for the last one will be read (default state).

The First Edge Hold function applies globally to all four capture timers.

Bit 2~0: Prescale Bits

Bit [2:0]	Capture Bits	LSB Step Size	Range
000	Bit[7:0] of free-running timer	1μ s	256μ s
001	Bit[8:1] of free-running timer	2μ s	512μ s
010	Bit[9:2] of free-running timer	4μ s	1024μ s
011	Bit[10:3] of free-running timer	8μ s	2048μ s
100	Bit[11:4] of free-running timer	16μ s	4096μ s

TABLE 7-6 Capture Prescaler

Address 28H : CLKCFG

Bits	Name	Description	Read	Write	Default
7	XTBUF[3]	XTBUF[3] : 1 : select port B interrupt, 0 :select port A interrupt	Yes	Yes	1'b1
6~5	XTBUF[2:1]	XBUT[2:1] DM, DP state 2'b11 Normal Drive SIE control 2'b10 DM Drive High, DP Drive Low 'K' State 2'b01 DM Drive Low, DP Drive High 'J' State 2'b00 DM Drive Low, DP drive Low SE0	Yes	Yes	2'b11
4	XTBUF[0]	XTBUF[0] : 1: When handshaking is ACK packet, the S/W generates interrupt for ENP1,2,3,4. 0: When handshaking is any packet, he S/W generates interrupt for ENP1,2,3,4.	Yes	Yes	1'b1
3	INSWDY	Internal clock switch to external clock delay time 1 : 4ms delay 0 : 128 us delay	Yes	Yes	0
2	INCODS	Internal clock output disable 1: Disable internal IRC clock output. XOUT pin will drive high. 0: Enable internal IRC clock output. The IRC clock is driven output to the XOUT pin.	Yes	Yes	0
1	EXOSEN	External Oscillator Enable 1:Enable the external oscillator. The clock is switched to external clock mode from IRC mode. 0:Disable Oscillator Enable	Yes	Yes	0
0	IRCEN	Internal IRC clock enable 1:Enable internal IRC clock. 0:Disable internal IRC clock.	Yes	Yes	1

Address 29,2AH : MPLL,NPLL

Address	Name	Description	Read	Write	Default
29H	MPLL[7:0]	Internal PLL parameter	Yes	Yes	00h
2AH	NPLL[7:0]	Internal PLL parameter PLL clock frequency : $f_{PLL} = (N[7:0]+1)/(M[7:0]+1) * f_{osc}$ Fosc : External oscillator or crystal clock frequency If Fosc is 6 Mhz , the initial PLL clock will be 48Mhz.	Yes	Yes	07h

Address 2B~2FH : General purpose Register

Bits	Name	Description	Read	Write	Default
7~0	Register	General purpose Register	Yes	Yes	00h

Address 30H~37H EP0 Received Buffer(EP0RX) **Rambnk[1:0] = 00 or 01**

Address	Description	Read	Write	Default
30H	Start address of EP0RX	Yes	Yes	XXh
30H~37H	Buffer length is 8 bytes for EP0RX	Yes	Yes	XXh

Address 38H~3FH EP0 Transmitter Buffer(EP0TX) **Rambnk[1:0] = 00 or 01**

Address	Description	Read	Write	Default
38H	Start address of EP0TX	Yes	Yes	XXh
38H~3FH	Buffer length is 8 bytes for EP0TX	Yes	Yes	XXh

Address 40H~47H EP1 Transmitter Buffer(EP1TX) **Rambnk[1:0] = 00 or 01**

Address	Description	Read	Write	Default
40H	Start address of EP1TX	Yes	Yes	XXh
40H~47H	Buffer length is 8 bytes for EP1TX	Yes	Yes	XXh

Address 48H~4FH EP2 Transmitter Buffer(EP2TX) **Rambnk[1:0] = 00 or 01**

Address	Description	Read	Write	Default
48H	Start address of EP2TX	Yes	Yes	XXh
48H~4FH	Buffer length is 8 bytes for EP2TX	Yes	Yes	XXh

Address 30H~3FH EP3 Transmitter Buffer0 (EP3TX0) **Rambnk[1:0] = 10**

Address	Description	Read	Write	Default
30H	Start address of EP3TX0	Yes	Yes	XXh
30H~3FH	Buffer length is 16 Bytes	Yes	Yes	XXh

Address 40H~4FH EP3 Transmitter Buffer1 (EP3TX1) **Rambnk[1:0] = 10**

Address	Description	Read	Write	Default
40H	Start address of EP3TX1	Yes	Yes	XXh
40H~4FH	Buffer length is 16 Bytes	Yes	Yes	XXh

Address 30H~3FH EP4 Received Buffer0 (EP4RX0) **Rambnk[1:0] = 11**

Address	Description	Read	Write	Default
30H	Start address of EP4RX0	Yes	Yes	XXh
30H~3FH	Buffer length is 16 Bytes	Yes	Yes	XXh

Address 40H~4FH EP4 Received buffer1 (EP4RX1) **Rambnk[1:0] = 11**

Address	Description	Read	Write	Default
40H	Start address of EP4RX1	Yes	Yes	XXh
40H~4FH	Buffer length is 16 Bytes	Yes	Yes	XXh

8.0 Instruction Set

Mnemonic, Operands	Description	Operation	Cycles	Status Affected
BCR R, bit	Clear bit in R	$0 \rightarrow R$	1	-
BSR R, bit	Set bit in R	$1 \rightarrow R$	1	-
BTRSC R, bit	Test bit in R, Skip if Clear	Skip if $R = 0$	$1/2^{(1)}$	-
BTRSS R, bit	Test bit in R, Skip if Set	Skip if $R = 1$	$1/2^{(1)}$	-
NOP	No Operation	No operation	1	-
CLRWDT	Clear Watchdog Timer	$00h \rightarrow$ WDT, $00h \rightarrow$ WDT prescaler	1	\overline{TO} , \overline{PD}
SLEEP	Go into power-down mode	$00h \rightarrow$ WDT, $00h \rightarrow$ WDT prescaler	1	\overline{TO} , \overline{PD}
RETURN	Return from subroutine	Top of Stack \rightarrow PC	2	-
RETFIE	Return from interrupt, set GIE bit	Top of Stack \rightarrow PC, $1 \rightarrow$ GIE	2	-
CLRA	Clear ACC	$00h \rightarrow$ ACC	1	Z
IOST R	Load IOST register	ACC \rightarrow IOST register	1	-
IOSTR R	Read IOST register	IOST register \rightarrow ACC	1	-
CLRR R	Clear R	$00h \rightarrow$ R	1	Z
MOVAR R	Move ACC to R	ACC \rightarrow R	1	-
MOVR R, d	Move R	$R \rightarrow$ dest	1	Z
DECR R, d	Decrement R	$R - 1 \rightarrow$ dest	1	Z
DECRSZ R, d	Decrement R, Skip if 0	$R - 1 \rightarrow$ dest, Skip if result = 0	$1/2^{(1)}$	-
INCR R, d	Increment R	$R + 1 \rightarrow$ dest	1	Z
INCRSZ R, d	Increment R, Skip if 0	$R + 1 \rightarrow$ dest, Skip if result = 0	$1/2^{(1)}$	-
ADDAR R, d	Add ACC and R	$R +$ ACC \rightarrow dest	1	C, DC, Z
SUBAR R, d	Subtract ACC from R	$R -$ ACC \rightarrow dest	1	C, DC, Z
ANDAR R, d	AND ACC with R	ACC and R \rightarrow dest	1	Z
IORAR R, d	Inclusive OR ACC with R	ACC or R \rightarrow dest	1	Z
XORAR R, d	Exclusive OR ACC with R	R xor ACC \rightarrow dest	1	Z
COMR R, d	Complement R	$\overline{R} \rightarrow$ dest	1	Z
RLR R, d	Rotate left f through Carry	$R<7> \rightarrow$ C, $R<6:0> \rightarrow$ dest<7:1>, C \rightarrow dest<0>	1	C
RRR R, d	Rotate right f through Carry	C \rightarrow dest<7>, $R<7:1> \rightarrow$ dest<6:0>, $R<0> \rightarrow$ C	1	C
SWAPR R, d	Swap R	$R<3:0> \rightarrow$ dest<7:4>, $R<7:4> \rightarrow$ dest<3:0>	1	-
MOVIA I	Move Immediate to ACC	$I \rightarrow$ ACC	1	-
ADDIA I	Add ACC and Immediate	$I +$ ACC \rightarrow ACC	1	C, DC, Z
SUBIA I	Subtract ACC from Immediate	$I -$ ACC \rightarrow ACC	1	C, DC, Z
ANDIA I	AND Immediate with ACC	ACC and I \rightarrow ACC	1	Z
IORIA I	OR Immediate with ACC	ACC or I \rightarrow ACC	1	Z

ATW

AT8PU86LV

Mnemonic, Operands	Description	Operation	Cycles	Status Affected
XORIA I	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z
RETIA I	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL I	Call subroutine	PC + 1 → Top of Stack, I → PC	2	-
GOTO I	Unconditional branch	I → PC	2	-

Note: 1. 2 cycles for skip, else 1 cycle

2. bit : Bit address within an 8-bit register R

R : Register address (00h to 7Fh)

I : Immediate data

ACC : Accumulator

d : Destination select;

=0 (store result in ACC)

=1 (store result in file register R)

dest : Destination

PC : Program Counter

PCHBUF : High Byte Buffer of Program Counter

WDT : Watchdog Timer Counter

GIE : Global interrupt enable bit

TO : Time-out bit

PD : Power-down bit

C : Carry bit

DC : Digital carry bit

Z : Zero bit

9.0 Clock Control

The chip can be generated clock from either IRC or from external crystal fed into PLL. The PLL clock can be programming 29h(MPLL), 2Ah(NPLL) register base on the external crystal frequency. For example code and steps as follows:

- (1) Power on, chip begins operation using the internal clock.
- (2) If user firmware sets Bit 1(EXOSCEN) of the CLKCFG(28h)register, the chip clock is from internal clock switching to external clock.

If external crystal use 12Mhz,the MPLL(29h) and MNPLL(2Ah) registers are needed to set 0h and 3h value.

$$f_{OSC} = 12\text{Mhz}, f_{PLL} \text{ need to equal } 48 \text{ Mhz}$$

$$f_{PLL} = (N[7:0]+1)/(M[7:0]+1) * f_{OSC} \dots \dots \dots (9.0-1)$$

From Eq.(9.0-1), we can get
 $N[7:0]=3, M[7:0]=0$

```

movia 0h // Load 0h to MPLL
movar MPLL
movia 3h // Load 3h to NPLL
movar NPLL
// set bit 1 high(external oscillator enable bit)
bsr CLKCFG,EXOSCEN_B
    
```

When setting EXTOSEN(28h-1 bit) is high, the USB/MCU clock is from internal clock switching to external clock.

- (3) The MCU clock switched to select clock are as follow : (MCU is 24Mhz)


```

BCR EPST1,CLKSW_B
BCR EPST1,SELCLK0_B
BCR EPST1,SELCLK1_B
BSR EPST1,CLKSW_B
// MCU clock switch to 16Mhz
BCR EPST1,CLKSW_B
BSR EPST1,SELCLK0_B
BCR EPST1,SELCLK1_B
BSR EPST1,CLKSW_B
// MCU clock switch to 12Mhz
            
```
- (4) After an addition delay the MCU is released to run. This delay depend on bit 3 of the CLKCFG(28h) register. The time is 128us if this bit is 0, or 4ms if this bit set 1. The timing(128us or 4ms) is internal clock switched to external clock.

10.0 Reset

There are three cases of reset on USB controller chip. These cases of reset occurrence are listed below.

1. Power On Reset Negative (PORN).
2. Watchdog Reset (WDR)
3. External Reset (EXR).

If the PORN,WDR, or EXR occurs, the chip will enter

reset status. The following events take place on reset status.

- (1) All registers are reset to their default values expect status registers.
- (2) The status register (03h) is reset to their default value only for PORN.
- (3) After reset status, program counter begins at address 0x0000.

PORN is asserted when VBUS(Vcc) voltage to the device is upper approximately 3.8V(see Figure 10-1).

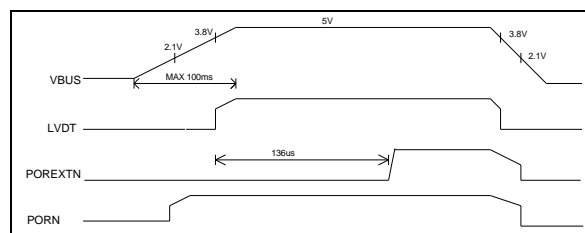


Figure 10-1 power on reset timing

11.0 Suspend Mode

The AT8PU86 chip has detection of resume and remote wake-up capability in suspend mode.

Normal code for entering suspend is shown below:

```

... Enable which PORTB wake-up
interrupt if desired for wake-up
bcr 12h,6 Clear resume bit
bsr 12h,7 Set suspend bit
sleep Chip go to sleep mode
    
```

More details on the various resume in suspend mode are given in the following sections.

11.1 Detection of Resume

The SIE uses the LineState(DP,DM) signals to determined when the USB transition from the 'J' to 'K' state in FS mode or from 'K' to 'J' state in LS mode.

When a device is suspended, a 'J'(FS) or 'K'(LS) state is on bus and SIE should be looking for whether a 'K'(FS) or 'J'(LS) state be forced on bus by HOST. If event is happened, the device is resumed by HOST.

11.2 Remote Wake-up

A device with remote wake-up capability must set PBIE register (09h) before into suspend mode. When PORTB[7:0] or PORTA[7:0] are any transition base on PBCON(0Ah) set in suspend mode, the device will start to remote wake-up function. And then, the device need set resume (12h,6) bit to send 'K' state (if FS mode) or 'J' state (if LS mode) remote signal. The remote signaling must be asserted (FS 'K' or LS 'J') at least 1ms for USB specification. The device don't clear resume bit until delay time at least 1ms or enter next suspend mode.

(1) Remote Wake-up on PB or PA interrupt

PBINTASK :

```
bcr USBMDCFG,SUSPMD_B
bcr INTFLAG,PBIF_B
```

```
//Device remove wake up host to sent J or K state
bsr USBMDCFG,RESMD_B
call delay_1ms
bcr USBMDCFG,RESMD_B
```

(2).Remote Wake-up on Watch-dog timeout

```
(a) WakeUp for Full_speed :
bcr CLKCFG,XTBUF[0]
call delay_1ms
bsr CLKCFG,XTBUF[0]
//Device remove wake up host to sent K state
```

```
(b) WakeUp for Low_speed:
bcr CLKCFG,XTBUF[1]
call delay_1ms
bsr CLKCFG,XTBUF[1]
//Device remove wake up host to sent J state
```

Note : (1) "J" state is DP= high(3.3V),DN=Low(0V);
 (2) "K" state is DP=Low(0V),DN=high(3.3V);
 on USB bus.

12.0 General Purpose I/O ports

Ports A are 8 bits I/O register. Ports B are 8 bits I/O register ,each bit can also selected as an external interrupt source for the microcontroller.

Figure 12-1 shows a diagram of a GPIO port pin. Refer Table7-2.1 and Table 7-2.2 , each pin can be independently configured as high-impedance inputs, inputs with internal pull-ups, open drain outputs, or traditional output s with selectable drive strength. When SPION(1fh,6) bit is set, the PA.4,PA.5,PA.6 and PA.7 pins are accessed by SPI hardware of chip. After reset, all GPIO data and controlled mode register is cleared, so the GPIO pins are as input mode.

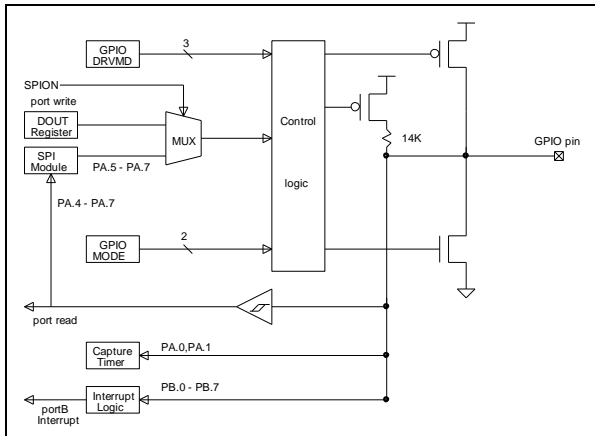


Figure 12-1 Block Diagram of GPIO port

3.0 USB and PS2 Mode Detection

The AT8PU86 are integrated USB and PS2 device on chip. When USB mode function is be enabled(set USBEN bit of PUMODE),the DP,DM can be read/write by SIE. The USB DP and DM pins can be used for PS2 SCLK and SDATA pins, respectively. When PS2 mode function is be enabled(set PS2EN bit of PUMODE), the SCLK and SDATA can be read/write at bits[1:0] of PORTC. The PS2 on chip support circuit is show Figure13-1.

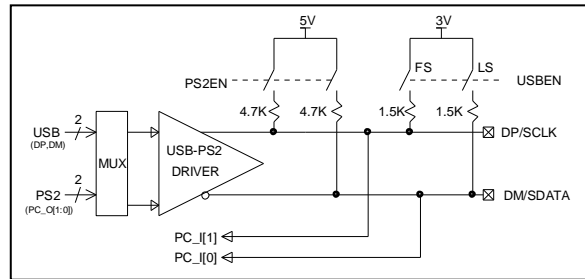


Figure13-1 Block diagram of USB/PS2 connections After power on reset(VBUS asserted < 100ms),user firmware need to detect PORTC[1:0] bits. For example code as follows:

```
movr PORTC,A
andia 03h // Detect portc[1:0]
btrsc STATUS,Z_B
goto SETUSB // USB mode
goto SETPS2 // PS2 mode
```

14.0 USB Transceiver

This block handles the USB signaling. This include features such as below.

1. Complies with USB Rev2.0
2. Support 12Mbits/s "Full Speed" and 1.5Mbits/s "Low speed".
3. Data and clock recovery from serial stream on the USB.
4. Build in pull-up 1.5k resistor.
5. Build in power-on reset.

14.1 USB Regulator output

The VREG pin provide a regulated output for internal USB transceiver and external supply power 3.3V chip.

5.0 USB Serial Interface Engine(SIE)

The SIE will handle the USB packets from/to transceiver and communication with the USB Host. Some key features of the USB SIE are :

1. For incoming packets, check CRC; For outgoing packets add CRC bytes.

2. Issue USB interrupt to the micro-controller only if IN/OUT token packets are successful transaction.
3. Automatic returned appropriate ACK/NAK/STALL handshake packets.
4. Automatic update the toggle bit (1/0) of data packet .
5. Handle the USB reset protocol; suspend condition detection; detection of resume; Handshake detection protocol.
6. SYNC/EOP generation and check.
7. Bit-stuffing/unstuffing.
8. Serializer/Deserialzer.

15.1 Default Control Endpoint : EP0

EP0 is the control transfer endpoint where the transmission is defined as the direction from device to host and receiving is defined as the direction from host to device. The EP0 buffers will be mapped into the shared SRAM buffer rather than dedicated FIFO.

15.2 Interrupt Transfer Endpoints : EP1 and EP2

The endpoint 1,2 is used for interrupt transmission(INT IN) .The maximum allowable interrupt data payload size 8 bytes for full-speed or low-speed transaction. The micro-controller needs to program the maximum packet size registers (15h-TX1CNT,16h-TX2CNT) properly to avoid any size errors. The interrupt transfer type is designed to support those devices that need to sent data infrequently but with bounded service period.

15.3 Bulk Transfer Endpoints:EP3 and EP4

The endpoint 3 is used for bulk transmission (BULK IN) and endpoint 4 is used for bulk receiving (BULK OUT). The maximum allowable bulk data payload size is 32 bytes for full-speed or low-speed transaction. The micro-controller needs to program the maximum packet size registers (17h-TX3CNT,18h-RX4CNT) properly to avoid any size errors. The bulk transfer type is designed to support devices that need to communicate relatively large amounts of data at highly variable times where the transfer can use any available bandwidth. The EP3 or EP4 buffer is stand-alone SRAM(32 bytes) that can be as general

purpose memory.

16.0 Micro-Controller

16.1 Timer0/Timer1

The Timer0/1 is a 8 bit clock counter with a programmable prescaler and a 8-bit overflow reload(T0RLD/T1RLD).The clock source of Timer0/1 comes from the internal clock(F_{MCUCLK}/4). The option of Timer0/1 precaler is defined by T0/1PS2,1,0(0Bh register) see Table 15-1.

T0/1 SP2, SP1, SP0	Prescaler Rate
3'b000	1*(4*clock)
3'b001	2*(4*clock)
3'b010	4*(4*clock)
3'b011	8*(4*clock)
3'b100	16*(4*clock)
3'b101	32*(4*clock)
3'b110	64*(4*clock)
3'b111	128*(4*clock)

Table 15-1 Timer0/1 Prescaler Rate

Timer1 also can be as a baud rate clock generator for the SPI module.

The Timer0/1 increment from 00h until it equals the T0RLD/T1RLD value. The timer interrupt flag(T0IF/T1IF) is asserted when the Timer0/1 rollover to 00h. The Timer0/1 also has corresponding interrupt enable bit(T0IE/T1IE). The Timer0/1 interrupt can be enabled/disabled by setting/clearing these bits. The Timer0/1 can be turned on and off by software control. When the Timer0/1 on control bit(0Bh,T0ON,T1ON) is set, the Timer0/1 increments from the clock source. When T0ON/T1ON is cleared, the Timer0/1 is turned off and cannot cause the Timer0/1 interrupt flag to be set. The Timer0/1 block diagram is show *Figure15-1*.

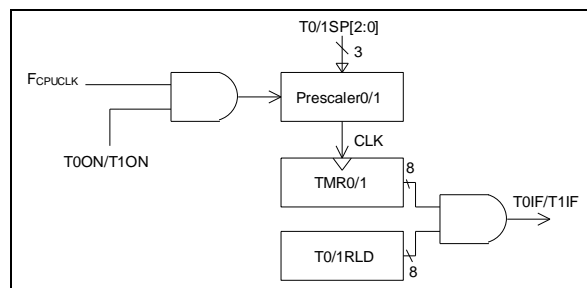


Figure15-1 Block diagram of Timer0/1

The Timer0/1 is calculated as follows:

```

MCU clock Fcpuclk= 6MHz
MOVIA    106D
MOVAR    T0RLD
MOVIA    0bH      (T0PS[2:0] = 011)
MOVAR    TMCON
    
```

T0IF = (106+1)*32*clock=570.667us

6.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on chip RC oscillator which does not require any external components. So the WDT will still run into SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset.

The CLRWDT instruction clears the WDT, if assigned to the WDT, and prevents it from timing out and generating a device reset.

The WDT can be disabled by clearing the control bit WDTE(08h-7). The WDT has a normal time-out period of 18ms(without prescaler). When the SLEEP instruction executes, the WDT and the prescaler will be reset.

The prescaler of WDT refers Table 7-4.

The block diagram of WDT shows in Figure 15-2.

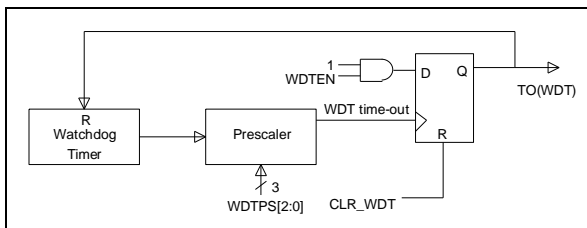


Figure 15-2 Block diagram of WDT

17. Capture Timer Register

Four 8-bit capture timer registers recode both rising and falling-edge timing value on two pins. The pinA.0 is capture in Timer A, and PinA.1 is capture in Timer B. These can be used latch the time at which a raising or falling event occurs at the pinA.0, pinA.1.

The block diagram of capture timer is show in Figure 16-1.

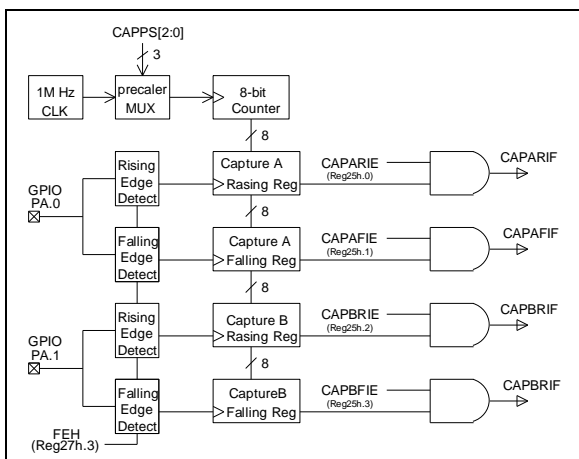


Figure 16-1 Block diagram of capture timer

The Prescaler see Table 7-6.

18.0 Serial Peripheral Interface (SPI)

The Serial Port Interface (SPI) module is a serial interface useful communication with other peripheral or micro-controller device.

The SPI module allows 8-bit of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used :

1. Serial Clock(SCK)
2. Serial Data IN (SDI)
3. Serial Data out (SDO)
4. Slave select(SSB)

The block diagram of SPI is show in Figure 17-1.

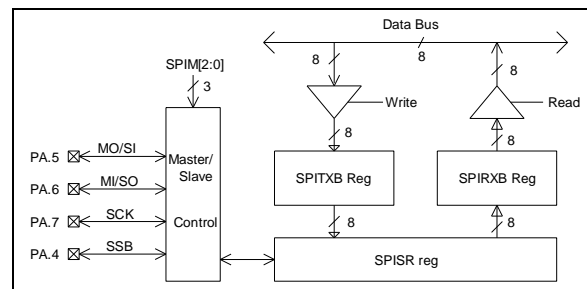


Figure 17-1 Block diagram of SPI

18.1 Master Mode

18.1.1 Master Mode with SSE Control(SSEMOD =0)

How to transmit/Receive data in this master mode , descript as below:

1. Enable SPI function by setting the SPION (1Fh-6) bit.
2. Decide the transmission rate and source by programming SPIM[2:0] bits. (Refer Table 7-5)
3. Write the data to SPITXB for transmitting if needed.
4. Set SSE (1Fh-4) bit to start transmit.
5. When the 8-bit data transmission starts, both of the SPITXIF and TXBFIF interrupt flags will set to 1. Beside, both of these are cleared by software. The TXBF flag also will be set to 1,cleared by software or by writing data to SPITXB register.
6. Write next byte data to SPITXB register before this byte transmission being finished if needed.
7. When the 8-bit data transmission is over, the SSE bit will be reset to "0" by hardware. Therefore, if user want to transmit/receive another 8-bit data user must set SSE bit to "1" again.
8. When the 8-bit data transmission is completed, the SPIRXIF interrupt flag will set to 1. Besides, the SPIRXIF is cleared by software. The RXBF

flag also will be set to “1”, cleared by software or by reading out SPRRXB register.

9. Read out the SPIRXB register before next byte transmission begin finished if needed.

The SPI mode timing is show in *Figure 18-1* for Master mode.

8.1.2 Master Mode without SSE Control(SSEMOD =1)

How to transmit/Receive data in this master mode , descript as below:

1. Enable SPI function by setting the SPION (1Fh-6) bit.
2. Decide the transmission rate and source by programming SPIM[2:0] bits.(Refer Table 7-5)
3. Write the data to SPITXB for transmitting if needed.
4. When the 8-bit data transmission starts, both of the SPITXIF and TXBFIF interrupt flags will set to 1. Beside, both of these are cleared by softwafe. The TXBF flag also will be set to 1,cleared by software or by writing data to SPITXB register.
5. Write next byte data to SPITXB register before this byte transmission being finished if next byte transmission is needed.
6. When the 8-bit data transmission is completed, the SPIRXIF interrupt flag will set to 1. Besides, the SPIRXIF is cleared by software. The RXBF flag also will be set to “1”, cleared by software or by reading out SPRRXB register.
7. Read out the SPIRXB register before next byte transmission begin finished if needed.

18.2 Slave Mode

18.2.1 Slave Mode with SSE Control(SSEMOD =0)

How to transmit/Receive data in this master mode , descript as below:

Enable SPI function by setting the SPION (1Fh-6) bit.

1. Enable/Disable the SSB pin control by programming SPIM[2:0] bits. (Refer Table 7-5)
2. Write the data to SPITXB for transmitting if needed.
3. Set SSE (1Fh-4) bit and wait the external clock pulses appear on SCK pin to start transmit.
4. When the 8-bit data transmission starts, both of the SPITXIF and TXBF interrupt flags will set to 1. Beside, both of these are cleared by software. The

TXBF flag also will be set to 1,cleared by software or by writing data to SPITXB register.

5. Write next new byte data to SPITXB register before this byte transmission being finished if next byte transmission is needed.
6. When the 8-bit data transmission is over, the SSE bit will be reset to “0” by hardware. Therefore, if user want to transmit/receive another 8-bit data user must set SSE bit to “1”, again before next clock pulse appearing SCK pin.
7. When the 8-bit data transmission completed, both of the SPIRXIF and RCBF interrupt flags will set to “1”. Besides, both of these bits are cleared by software. The RXBF flag also will be set to “1”, cleared by software or by reading out SPIRXB register.
8. Read out the SPIRXB register before next byte transmission begin finished if needed.

The SPI mode timing is show in *Figure 18-2* for Salve mode.

18.2.2 Slaver Mode with SSE Control(SSEMOD =1)

1. Enable SPI function by setting the SPION (1Fh-6) bit.
2. Enable/Disable the SSB pin control by programming SPIM[2:0] bits. (Refer Table 7-5)
3. Write the data to SPITXB for transmitting if needed.
4. Wait the external clock pulses appear on SCK pin to start transmit.
5. When the 8-bit data transmission starts, both of the SPITXIF and TXBFIF interrupt flags will set to 1. Beside, both of these are cleared by software. The TXBF flag also will be set to 1,cleared by software or by writing data to SPITXB register.
6. Write next new byte data to SPITXB register before this byte transmission being finished if next byte transmission is needed
7. When the 8-bit transmission is completed, both the SPIRXIF and RXBF interrupt flags will be set to 1. Besides, both of these bits are cleared by software. The RXBF flag also will be set to 1, cleared by software or by reading out SPITXB register.
8. Read out the SPIRXCB register before next byte transmission begin finished if needed.

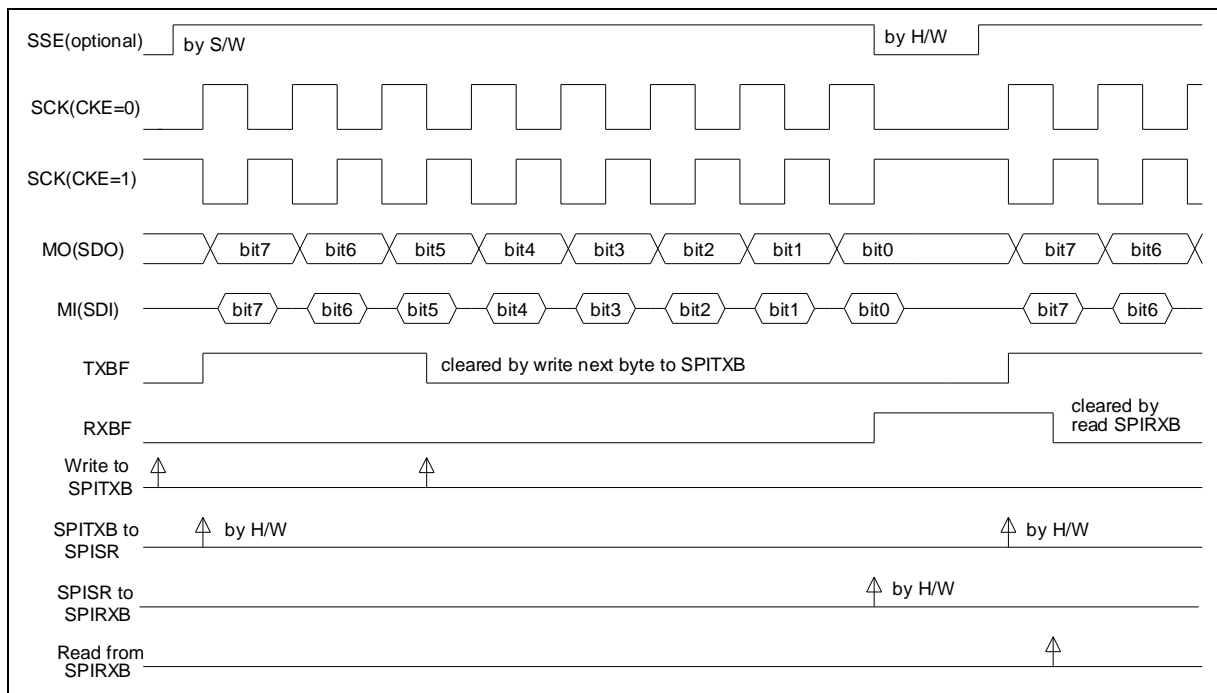


Figure 18-2 SPI Mode Timing (Master Mode)

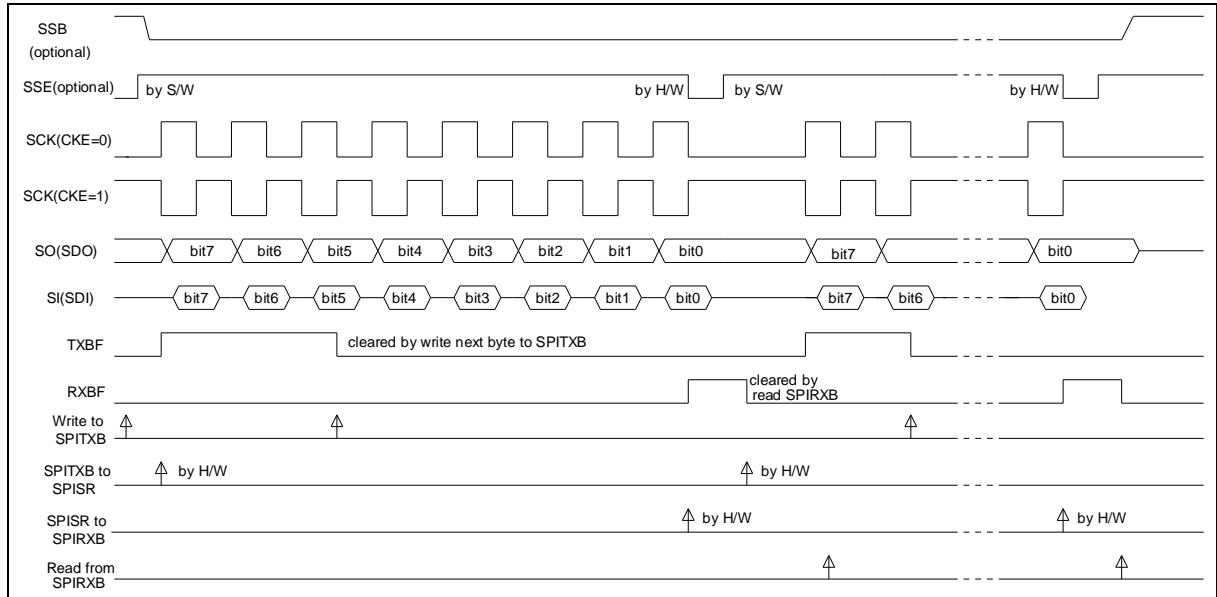


Figure 18-2 The SPI mode Timing (Slave Mode, with SSB control enable/disable)

19. SPI communication code

The following code can be used to implement the SPI data communication:

```

bcr SPICON,SPIM0_B // SPIM[2:0]=3'b011 , set SPI as master mode and clock=Fcpu/16
bsr SPICON,SPIM1_B
bsr SPICON,SPIM2_B
bsr SPICON,SPION_B //Enable SPI mode
bsr SPICON,CKEDG_B // SPI clock falling edge sent Data and raising edge sample data
    
```

Subroutine for SPI transmitted code

SPI_TX :

```

bcr    SPISTAT,SDOOD_B // MO(PA.5) normal Drive
movr   ADDRESS,A      // Will sent data(address) to save ACC
movar  SPITXB          // Acc data move to SPITXB buffer
bsr    SPICON,SSE_B   // Asserted SSE (start to transmitted)
WAITSEN : btrsc SPICON,SSE_B // Wait transmitted to end
        goto    WAITSEN
        return

```

Subroutine for SPI received code

SPI_RX:

```

bsr    SPISTAT,SDOOD_B // SDO open drain
movia  ffh              // When MO(PA.5) are connected to MI(PA.6), the SDO
                          // need pull-high in received .

movar  SPITXB
bcr    SPISTAT,RXBF_B
bsr    SPICON,SSE_B   // Asserted SSE (start to received)
WAITRXB: btrsc SPISTAT,SSE_B // wait received interrupt
        goto    WAITRXB
bcr    SPISTAT,RXBF_B // Clear RXBF bit
        return

```

20. Interrupt

The AT8PU86 has interrupt as following:

1. Timer 0 match interrupt.
2. Timer 1 match interrupt.
3. SPI transmit module interrupt.
4. SPI receive module interrupt.
5. Capture Timer A interrupt.
6. Capture Timer B interrupt.
7. GPIO(PORTB0~7) or GPIO(PORTA0~7) external interrupt.
8. USB bus reset interrupt.
9. USB resume interrupt.
10. USB suspend interrupt.
11. USB endpoint0,1,2,3 and 4 interrupt.
12. USB SOF interrupt.

The AT8PU86LV reset vector is fixed at 0x0000h and the interrupt vector is at 0x0003h.

A global interrupt enable bit, GIE(Reg.0Ch-7), enable(if set) all un-masked interrupts or disables(if cleared) all interrupts. Individual interrupts can be enable/disable through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.

The interrupt priority is decided by customer firmware control.

20. Absolute Maximum Ratings

Parameter	Conditions	Values		Unit
		min.	max.	
Ambient Operating Temperature	-	-10	85	°C
Storage Temperature	-	-10	150	°C
DC Supply Voltage	-	2.4	5.5	V
Supply Current	-	-	-	mA

21. DC Characteristics (Operating Temperature = 0 to 70 °C)

21.1 General

Symbol	Parameter	Conditions	Values		Unit
			min.	max.	
V _{CC}	Operating Voltage	-	4.5	5.5	V
I _{CC1}	Operating Voltage Current Typical = mA ^[1]	V _{CC} =5.5V, No GPIO loading IRC Operating, MCU=12MHz	-	13	mA
I _{CC2}	Operating Voltage Current Typical = mA ^[1]	V _{CC} =5.5V, No GPIO loading IRC Operating, MCU=24MHz	-	17	mA
I _{CC3}	Operating Voltage Current(EXOSC) Typical = mA ^[1] extern crystal =12MHz	V _{CC} =5.5V, No GPIO loading PLL Operating, MCU=12MHz	-	14	mA
I _{CC4}	Operating Voltage Current(EXOSC) Typical = ^[1] extern crystal =12MHz	V _{CC} =5.5V, No GPIO loading PLL Operating, MCU=24MHz	-	18	mA
I _{CC5}	Operating Voltage Current (Disable USB module)	V _{CC} =5V, No GPIO loading IRC Operating, MCU=24MHz		12	mA
I _{CC6}	Operating Voltage Current (Disable USB module)	V _{CC} =5V, No GPIO loading IRC Operating, MCU=12MHz		8	mA
I _{CC7}	Operating Voltage Current (Disable USB module)	V _{CC} =3.3V, No GPIO loading IRC Operating, MCU=24MHz		6	mA
I _{CC8}	Operating Voltage Current (Disable USB module)	V _{CC} =3.3V, No GPIO loading IRC Operating, MCU=12MHz		4	mA
I _{SPD}	Suspend Current(enable or disable USB)	With IRC(17us)	-	100	uA
V _{POR}	Power on Reset		2.0	-	V
V _{LVDT}	Low voltage detect		3.8		V
T _{VBUSST}	Vbus Power on Slew Time	Linear ramp:0 to 4V		100	ms
V _{REG}	VREG Regulator output	-	3.0	3.6	V
I _{REG}	VREG supply current			45	mA

21.2 GPIO Interface

Symbol	Parameter	Conditions	Values		Unit
			min.	max.	
RUP	Pull-up Resistor	-	11.6	13.7	K Ω
V _{OL_HD5V}	Output Low Voltage(High drive)	OVDD=5V,I _{OL} =20mA	-	0.8	V
V _{OL_HD3V}	Output Low Voltage(High drive)	OVDD=3.3V, I _{OL} =16mA	-	0.8	V
V _{OL_MD5V}	Output Low Voltage(Medium drive)	OVDD=5V,I _{OL} =5.5mA	-	0.4	V
V _{OL_MD3V}	Output Low Voltage(Medium drive)	OVDD=3.3V,I _{OL} =4mA	-	0.4	V
V _{OL_LD5V}	Output Low Voltage(Low drive)	OVDD=5V,I _{OL} =2mA	-	0.4	V
V _{OL_LD3V}	Output Low Voltage(Low drive)	OVDD=3.3V,I _{OL} =1.5mA	-	0.4	V
V _{OH}	Output High Voltage	OVDD =5V,I _{OH} =2mA	OVDD-2	-	V
V _{OH}	Output High Voltage	I _{OH} =2mA	OVDD-1	-	V
V _{IL}	Input Threshold Voltage	High to Low edge, Port A,B	0.4*OVDD	0.6*OVDD	V
V _{IH}	Input Threshold Voltage	Low to High edge,PortA,B	0.4*OVDD	0.6*OVDD	V

Note:

[1]:Bench measurements on nominal operating conditions. V_{cc} = Vbus

22. AC Characteristics

22.1 Clock Period

Symbol	Parameter	Conditions	Values		Unit
			min.	max.	
F _{IRC1}	Internal Clock Frequency	Internal Clock Enable;	24-0.25%	24+0.25%	MHz
F _{EXO}	External Clock Frequency	External clock enable; PLL operating	48-0.25%	48+0.25%	MHz

22.2 USB Timing

Symbol	Parameter	Conditions	Values		Unit
			min.	max.	
T _R	Transition Rise Time	C _{load} =200pF(10%~90%)	-	-	ns
T _R	Transition Rise Time	C _{load} =600pF(10%~90%)	-	-	ns
T _F	Transition Fall Time	C _{load} =200pF(10%~90%)	-	-	ns
T _F	Transition Fall Time	C _{load} =600pF(10%~90%)	-	-	ns
V _{CRS}	Output Signals Crossover	C _{load} =200 to 600 pF	1.3	2.0	V

Note: See Figure 21-2

22.3 SPI Timing

Symbol	Parameter	Conditions	Values		Unit
			min.	max.	
T _{SMCK}	SPI Master Clock Rate	-	-	12	Mhz
T _{SSCK}	SPI Slave Clock Rate	-	-	12	Mhz
T _{SCKH}	SPI Clock High Time	-	41.65	-	ns
T _{SCKL}	SPI Clock Low Time	-	41.65	-	ns
T _{MDY}	Master Data out Delay Time	-	5	-	ns
T _{MSU}	Mater Input Data Set-up Time	-	10	-	ns
T _{MHD}	Master Input Data Hold Time	-	2	-	ns
T _{SDY}	Slave Data out Delay Time	-	5	-	ns
T _{SSU}	Slave Input Data Set-up Time	-	10	-	ns
T _{SHD}	Slave Input Data hold Time	-	2	-	ns
T _{SSBSU}	Slave Select Bar Set-up Time	-	10	-	ns
T _{SSBHD}	Slave Select Bar hold Time	-	10	-	ns

Note: See Figure 21-3, Figure 21-4

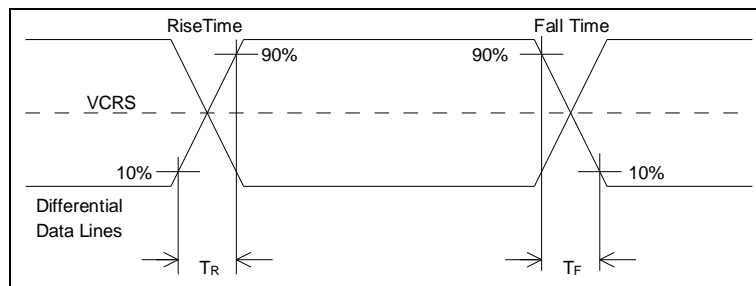


Figure 21-2 USB Data Signal Rise and Fall Time

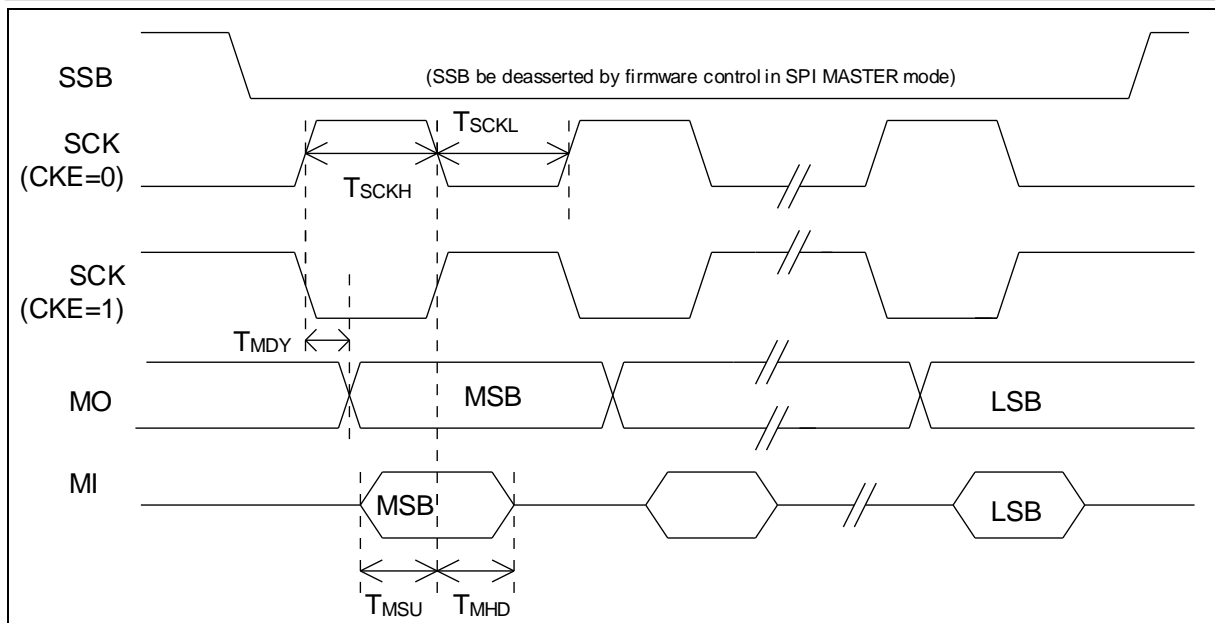


Figure 21-3 SPI Master Timing

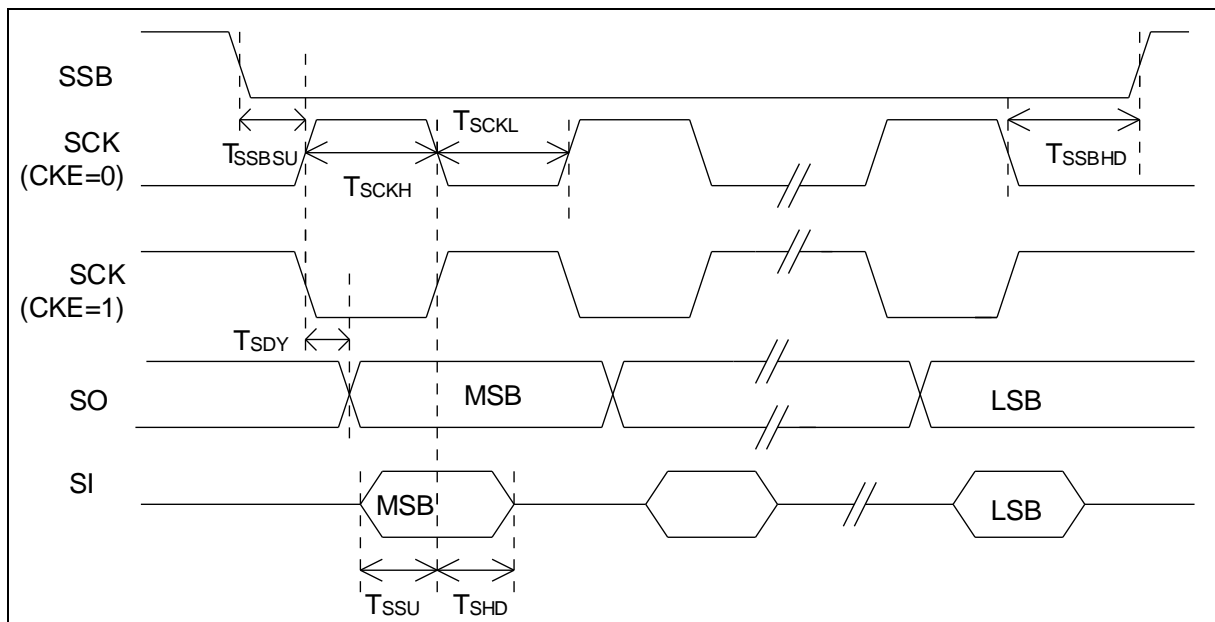
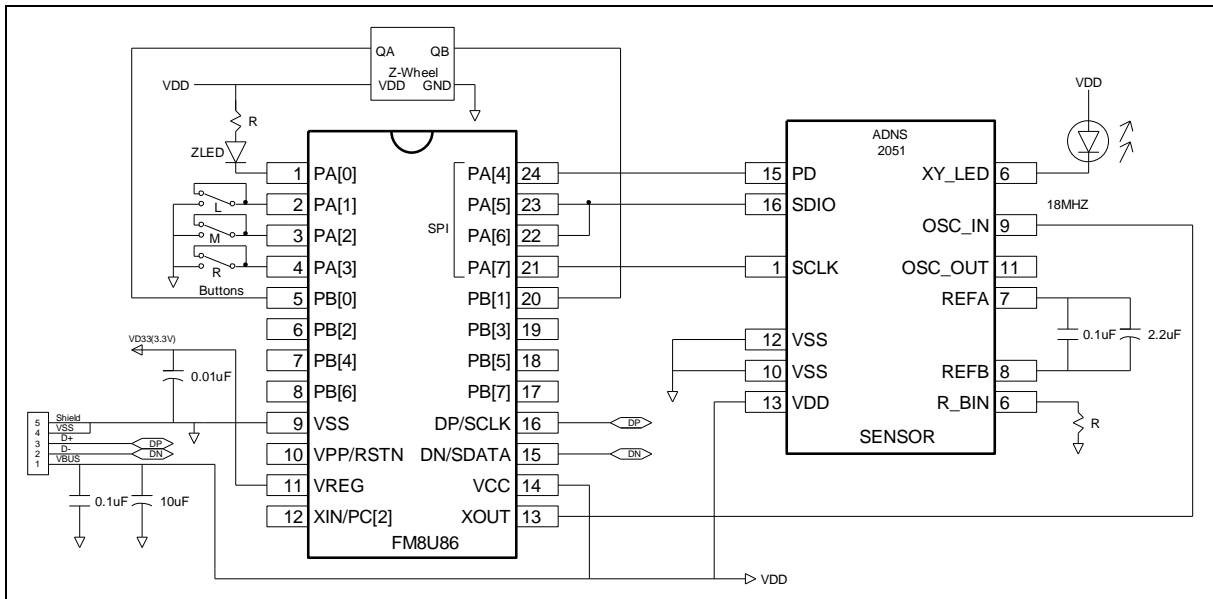


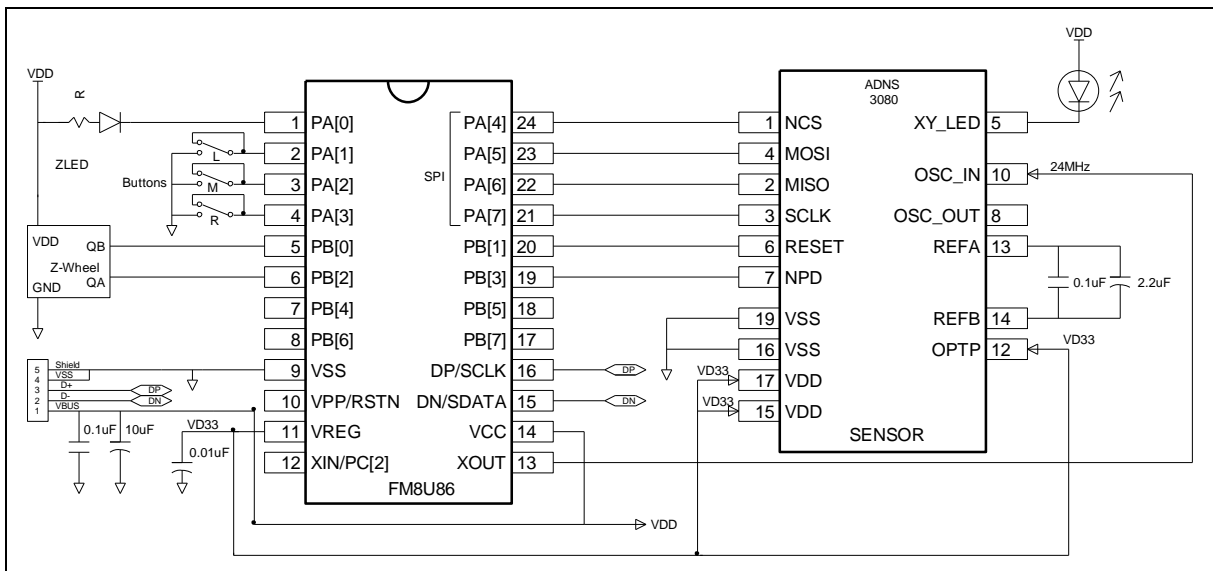
Figure 21-4 SPI Slave Timing

23.0 Application Circuit

- **AT8PU86LV Mechanical Z/2 3D3Key Application , without supply clock and power to Sensor.**



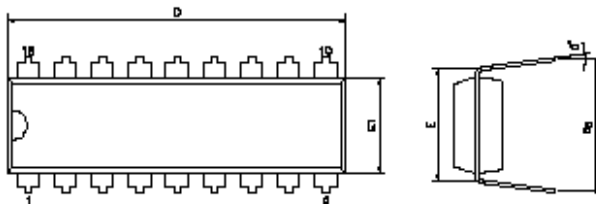
- **AT8PU86LV Mechanical Z/2 3D3Key Application, with supply clock(24MHz) and power(3.3V) to Sensor.**



Note: Subject VREG connect 10uf capacitance to VSS

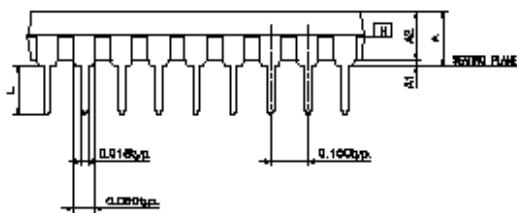
24.0 Package Diagrams

■ 18- LEAD (300mil) DIP



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	0.880	0.900	0.920
E	0.300 BSC.		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
ϕ_B	0.335	0.355	0.375
ϕ^*	0	7	15

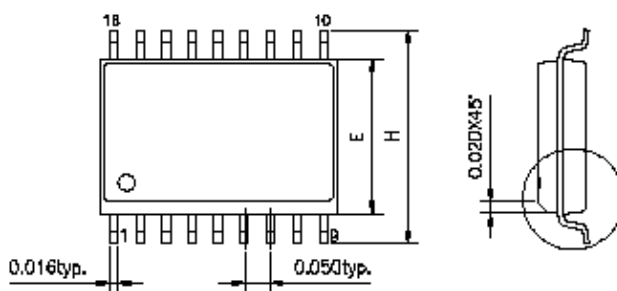
UNIT : INCH



NOTES:

1. JEDEC OUTLINE : MS-001 AC
2. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. ϕ_B IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EDGE INTERDIGIT.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE \square COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

■ 18- LEAD (300mil) SOP

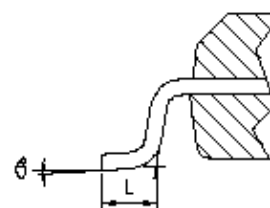
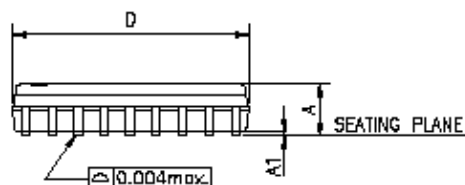


SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.447	0.463
E	0.281	0.299
H	0.394	0.419
L	0.016	0.050
ϕ^*	0	8

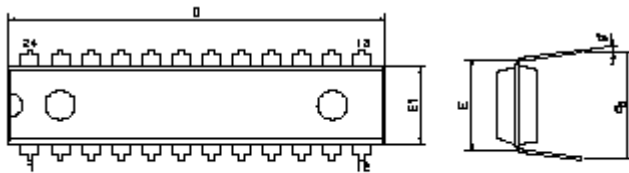
UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-013 AB
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.008in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

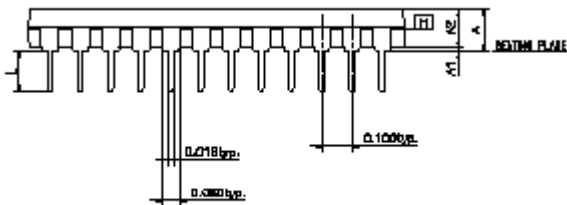


■ 24- LEAD (300mil) DIP



SYMBOLS	MIN.	NOM.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.230	1.250	1.280
E	0.300 BSC.		
E1	0.253	0.258	0.263
L	0.115	0.130	0.150
E_p	0.335	0.355	0.375
ϕ	0	7	15

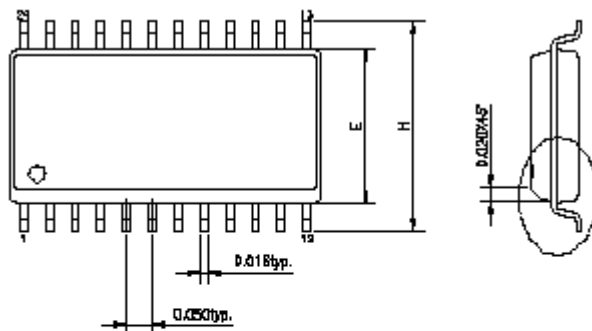
UNIT : INCH



NOTES:

1. JEDEC OUTLINE : MS-001 AF
2. "D", "E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.10 INCH.
3. E_p IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO CASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MINIMUM.
6. DATUM PLANE (A) COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

■ 24- LEAD (300mil) SOP

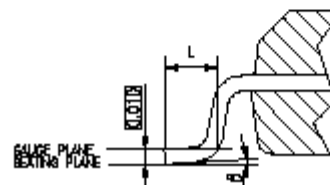
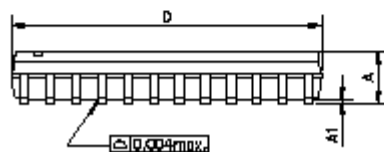


SYMBOLS	MIN.	NOM.	MAX.
A	—	—	0.104
A1	0.004	—	—
D	0.599	0.600	0.624
E	0.291	0.295	0.299
H	0.394	0.405	0.419
L	0.016	0.035	0.050
ϕ	0	4	8

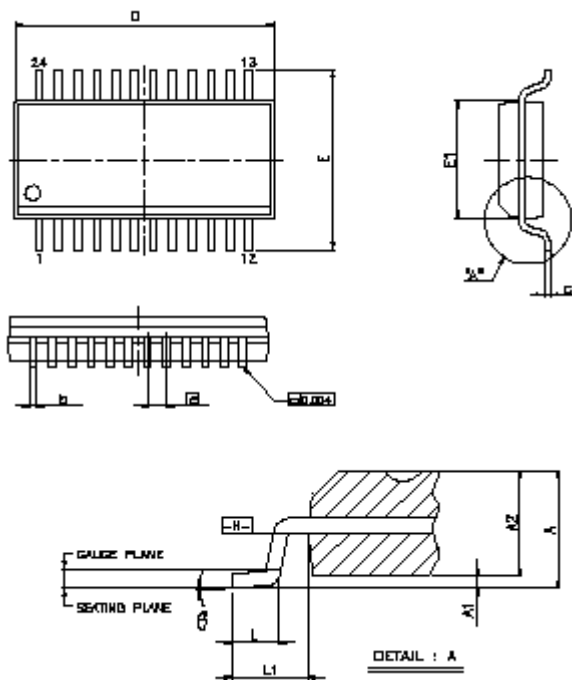
UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-119 AA
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.



■ 24_LEAD SSOP



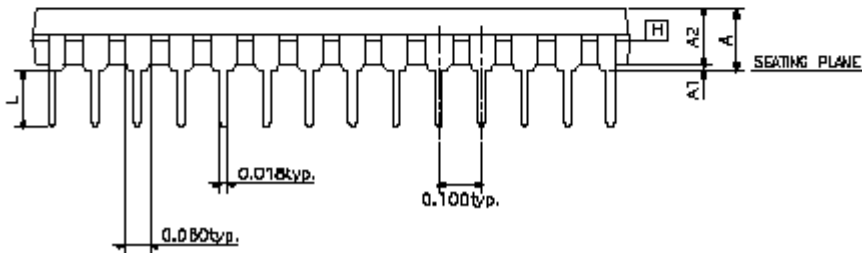
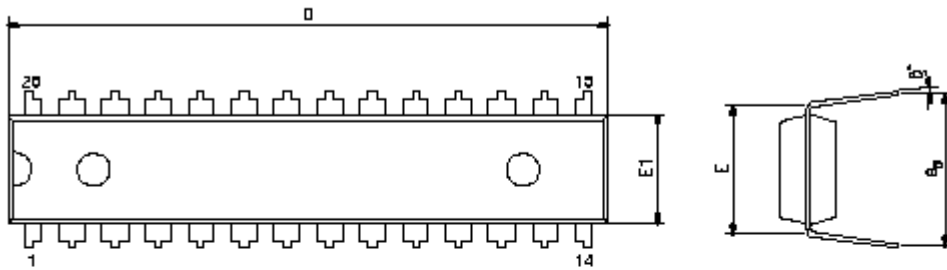
SYMBOLS	MIN.	NOM.	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	-	-	0.050
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
b	0.008	-	0.012
C	0.007	-	0.010
Ⓜ	0.025 BASIC		
L	0.016	0.025	0.050
L1	0.041 BASIC		
Ⓢ	Ⓢ	-	Ⓢ

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MO-137 AE
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.008" PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.010" PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.004" TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.002" AT LEAST.

■ 28- LEAD (300mil) DIP



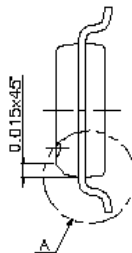
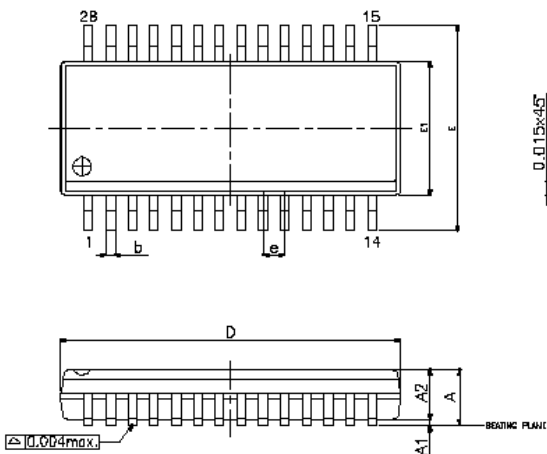
SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
e _P	0.330	0.350	0.370
θ°	0	7	15

UNIT : INCH

NOTE:

1. JEDEC OUTLINE : MS-015 AH

■ 28- LEAD (300mil) SSOP

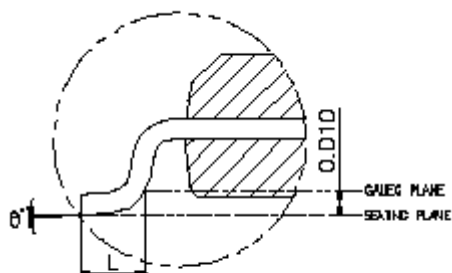


SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	-	0.059
b	0.008	0.012
D	0.386	0.394
E1	0.150	0.157
e	0.025 BASIC	
E	0.228	0.244
L	0.016	0.050
θ*	0	θ

UNIT : INCH

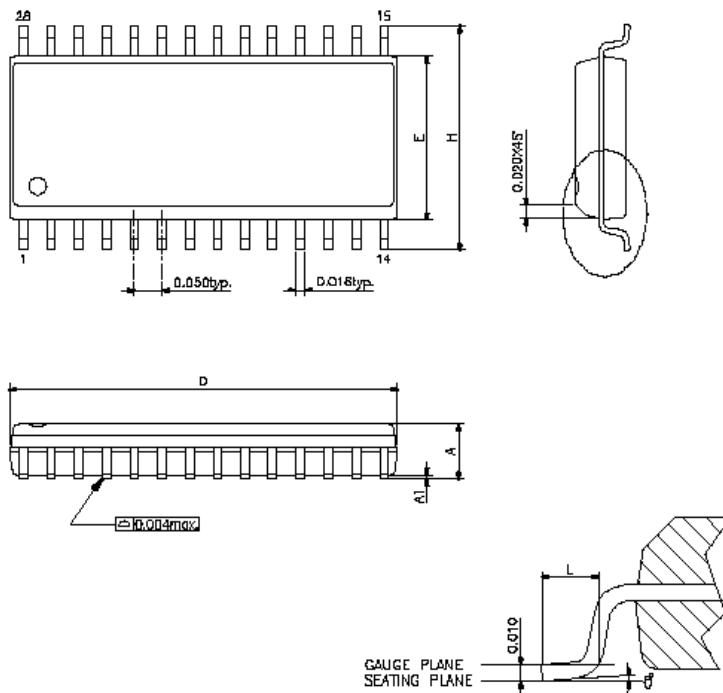
NOTES:

- JEDEC OUTLINE : MO-137 AF
- DIMENSIONS "D" DOES NOT INCLUDE WELD FLASH, PROTRUSIONS OR GATE BURRS. WELD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (0.006in) PER SIDE.
- DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm (0.010in) PER SIDE.



DETAIL A

■ 28- LEAD (300mil) SOP



SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.697	0.713
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
Ø	0	8

UNIT : INCH

NOTES:

1. JEDEC OUTLINE : MS-013 AE
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.