ATW

AT8A22

EPROM/ROM-Based 8-Bit Microcontroller Series

Devices Included in this Data Sheet:

- AT8A22E : EPROM devices
- AT8A22 : Mask ROM devices

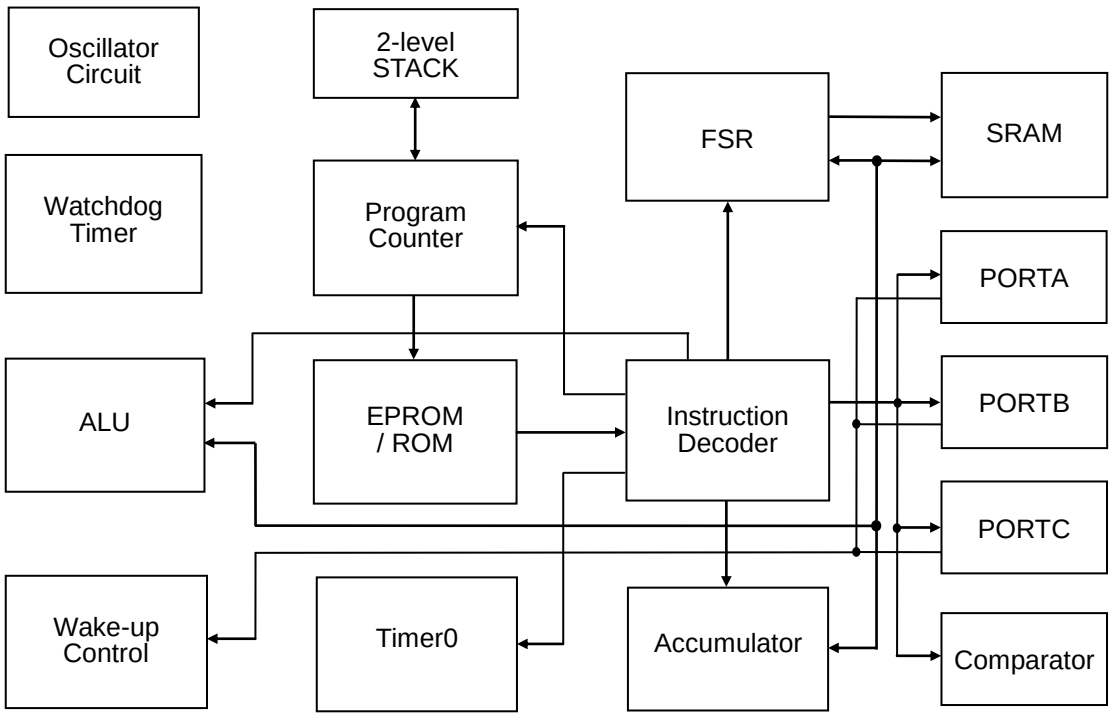
FEATURES

- Only 38 single word instructions
- All instructions are single cycle except for program branches which are two-cycle
- 13-bit wide instructions
- All ROM/EPROM area GOTO/LGOTO instruction
- All ROM/EPROM area subroutine CALL/LCALL instruction
- 8-bit wide data path
- 2-level deep hardware stack
- 1K x 13 bits on chip EPROM/ROM
- 72 x 8 bits on chip general purpose registers (SRAM)
- Operating speed: DC-20 MHz clock input
  DC-100 ns instruction cycle
- 4 channel comparator
- 1 channel IR output with programmable frequency and duty cycle
- Direct, indirect addressing modes for data accessing
- 8-bit real time clock/counter (Timer0) with 8-bit programmable prescaler
- Internal Power-on Reset (POR)
- Built-in Low Voltage Detector (LVD) for Brown-out Reset (BOR)
- Power-up Reset Timer (PWRT) and Oscillator Start-up Timer(OST)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation and soft-ware watch-dog enable/disable control
- Three I/O ports IOA , IOB and IOC with independent direction control
- Wake-up from SLEEP by Port IOA/IOB/IOC input status change
- Power saving SLEEP mode
- Programmable Code Protection
- Selectable oscillator options:
  - ERC: External Resistor/Capacitor Oscillator
  - HF: High Frequency Crystal/Resonator Oscillator
  - XT: Crystal/Resonator Oscillator
  - LF: Low Frequency Crystal Oscillator
  - IRC: Internal Resistor/Capacitor Oscillator (455KHz)
  - ERIC: External Resistor/Internal Capacitor Oscillator
- Wide-operating voltage range:
  - EPROM : 2.3V to 5.5V
  - ROM : 2.3V to 5.5V

GENERAL DESCRIPTION

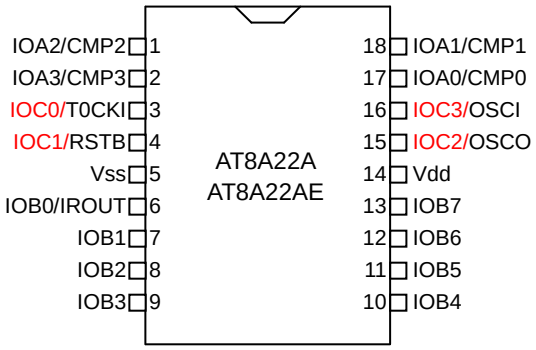
The AT8A22 series is a family of low-cost, high speed, high noise immunity, EPROM/ROM-based 8-bit CMOS microcontrollers. It employs a RISC architecture with only 38 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.
The AT8A22 series consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Oscillator Start-up Timer(OST), Watchdog Timer, EPROM/ROM, SRAM, tri-state I/O port, Power saving SLEEP mode, real time programmable clock/counter, Wake-up from SLEEP mode, and Code Protection for EPROM products. There are three oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator.
The AT8A22 address 1K×13 of program memory.
The AT8A22 can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory.

BLOCK DIAGRAM

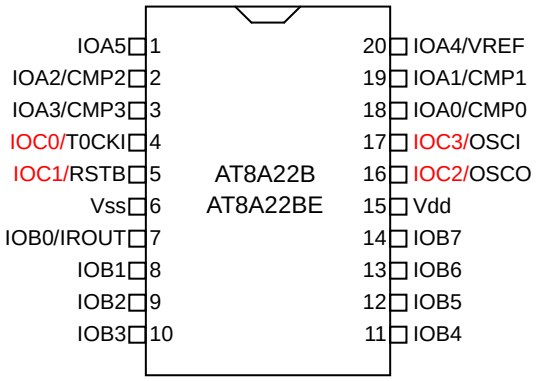


PIN CONNECTION

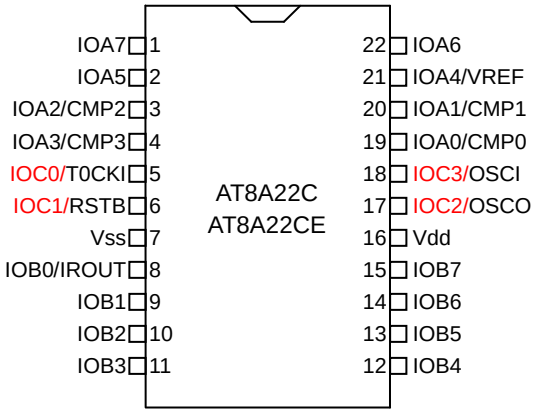
PDIP, SOP



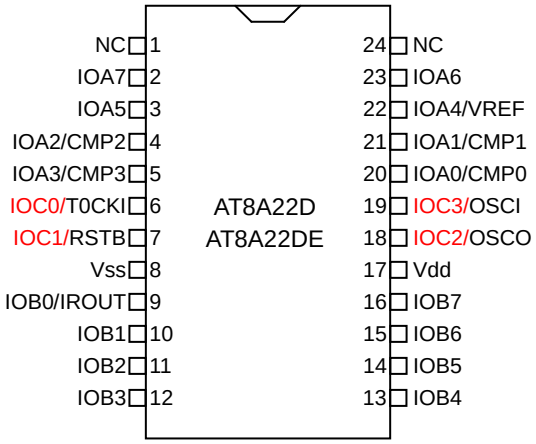
PDIP, SOP



SKINNY PDIP



SOP



PIN DESCRIPTIONS

Name	I/O	Description
IOA0 ~ IOA7	I/O	Bi-direction I/O pins with system wake-up function Comparator input pins
IOB0 ~ IOB7	I/O	Bi-direction I/O pins with system wake-up function
IOC0 ~ IOC3	I/O	Bi-direction I/O port, and IOC1 is an input only pin.
CMP0 ~ CMP3	I	Comparator input pins
VREF	I	Comparator VREF input pin
IROUT	O	IR carrier output pin
T0CKI	I	Clock input to Timer0. Must be tied to Vss or Vdd, if not in use, to reduce current consumption
RSTB	I	System clear (RESET) input. This pin is an active low RESET to the device.
OSCI	I	X'tal type: Oscillator crystal input RC type: Clock input of RC oscillator
OSCO	O	X'tal type: Oscillator crystal output. RC mode: Outputs with the instruction cycle rate
Vdd	-	Positive supply
Vss	-	Ground

Legend: I=input, O=output, I/O=input/output

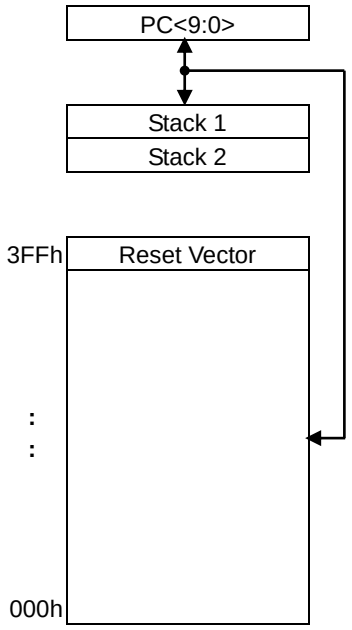
1.0 MEMORY ORGANIZATION

AT8A22 memory is organized into program memory and data memory.

1.1 Program Memory Organization

The AT8A22 have a 10-bit Program Counter (PC) capable of addressing a 1K×13 program memory space.
The RESET vector for the AT8A22 is at 3FFh.
AT8A22 supports all ROM/EPROM area **LCALL**/**LGOTO** instructions without page.

FIGURE 1.1: Program Memory Map and STACK



AT8A22/22E

1.2 Data Memory Organization

Data memory is composed of Special Function Registers and General Purpose Registers.
The General Purpose Registers are accessed either directly or indirectly through the FSR register.
The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device.
In AT8A22/22E, the data memory is partitioned into two banks. Switching between these banks requires the RP0 bit in the FSR register to be configured for the desired bank.

TABLE 1.1: Registers File Map for AT8A22/22E Series

FSR<6> / Address	Description	
	0 (Bank 0)	1 (Bank 1)
00h	INDF	Memory back to address in Bank 0
01h	TMR0	
02h	PCL	
03h	STATUS	
04h	FSR	
05h	PORTA	
06h	PORTB	
07h	PORTC	
08h | 0Fh	General Purpose Registers	
10h | 2Fh	General Purpose Registers	
30h | 3Fh	General Purpose Registers	General Purpose Registers

NA	OPTION
05h	IOSTA
06h	IOSTB
07h	IOSTC
08h	CMPCON
09h	PCON
0Ah	AWUCON
0Bh	BWUCON
0Ch	CWUCON
0Dh	IRCYCLE
0Eh	IRDUTY

TABLE 1.2: The Registers Controlled by OPTION or IOST Instructions

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (w)	OPTION	-	T0CS1	T0CS0	T0SE	PSA	PS2	PS1	PS0
05h (w)	IOSTA	Port A I/O Control Register							
06h (w)	IOSTB	Port B I/O Control Register							
07h (w)	IOSTC	-	-	-	-	Port C I/O Control Register			
08h (w)	CMPCON	GP3	CMPON	VREF1	VREF0	C3ON	C2ON	C1ON	C0ON
09h (w)	PCON	WDTE	-	LVDTE	-	-	IROEN	IRSC	IREN
0Ah (w)	AWUCON	WUA7	WUA6	WUA5	WUA4	WUA3	WUA2	WUA1	WUA0
0Bh (w)	BWUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0
0Ch (w)	CWUCON	-	-	-	-	WUC3	WUC2	WUC1	WUC0
0Dh (w)	IRCYCLE	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
0Eh (w)	IRDUTY	IRD7	IRD6	IRD5	IRD4	IRD3	IRD2	IRD1	IRD0

TABLE 1.3: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
01h (r/w)	TMR0	8-bit real-time clock/counter							
02h (r/w)	PCL	Low order 8 bits of PC							
03h (r/w)	STATUS	GP2	GP1	GP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04h (r/w)	FSR	*	RP0	Indirect data memory address pointer					
05h (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
06h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
07h (r/w)	PORTC	-	-	-	-	IOC3	IOC2	IOC1	IOC0

Legend: - = unimplemented, read as '0', * = unimplemented, read as '1',

2.0 FUNCTIONAL DESCRIPTIONS

2.1 Operational Registers

2.1.1 INDF (Indirect Addressing Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							

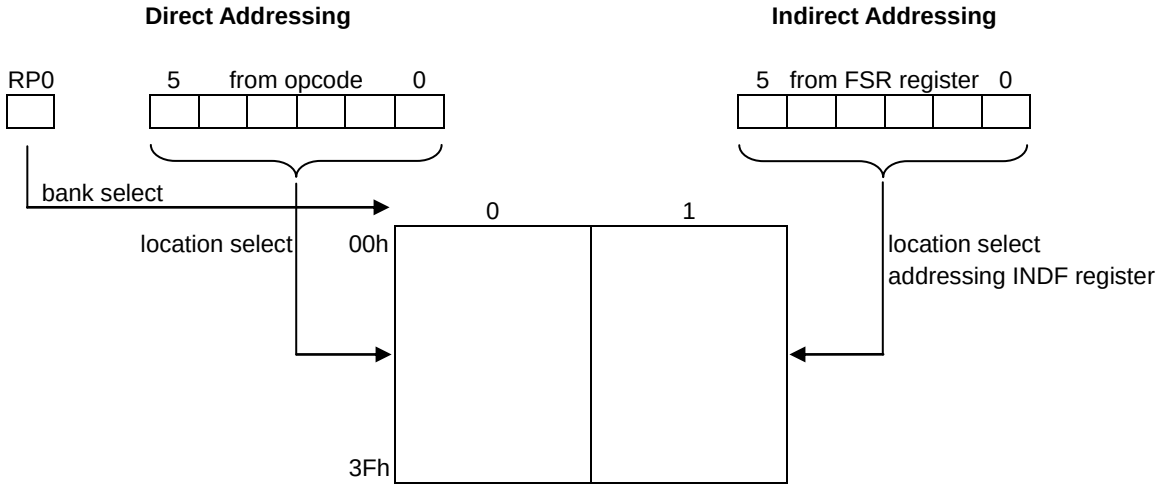
The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0") will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).
The bits 5-0 of FSR register are used to select up to 64 registers (address: 00h ~ 3Fh).
In AT8A22/22E, the data memory is partitioned into two banks. Switching between these banks requires the RP0 bit in the FSR register to be configured for the desired bank. The lower locations of each bank are reserved for the Special Function Registers. Above the Special Function Registers are General Purpose Registers. All Special Function Registers and some of General Purpose Registers from other banks are mirrored in bank 0 for code reduction and quicker access.

Accessed Bank	RP0
0	0
1	1

EXAMPLE 2.1: INDIRECT ADDRESSING

- Register file 38 contains the value 10h
- Register file 39 contains the value 0Ah
- Load the value 38 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (@FSR=39h)
- A read of the INDR register now will return the value of 0Ah.

FIGURE 2.1: Direct/Indirect Addressing for AT8A22/22E



2.1.2 TMR0 (Time Clock/Counter register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
01h (r/w)	TMR0	8-bit real-time clock/counter							

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the instruction cycle clock or by an external clock source (T0CKI pin) defined by T0CS bit (OPTION<5>). If T0CKI pin is selected, the Timer0 is increased by T0CKI signal rising/falling edge (selected by T0SE bit (OPTION<4>)).
The prescaler is assigned to Timer0 by clearing the PSA bit (OPTION<3>). In this case, the prescaler will be cleared when TMR0 register is written with a value.

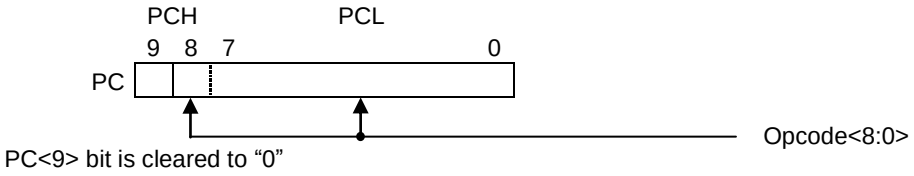
2.1.3 PCL (Low Bytes of Program Counter) & Stack

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
02h (r/w)	PCL	Low order 8 bits of PC							

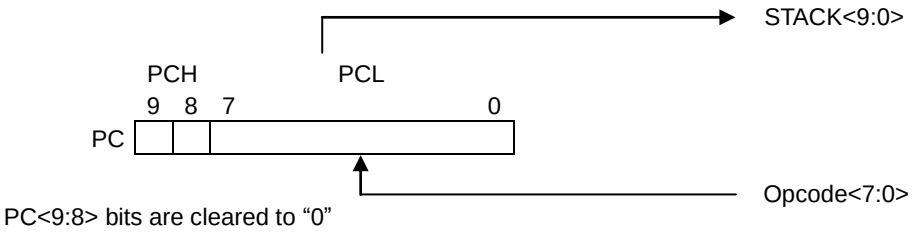
AT8A22 devices have a 10-bit wide Program Counter (PC) and two-level deep 10-bit hardware push/pop stack. The low byte of PC is called the PCL register and which contains the PC<7:0> bits. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<9:8> bit and is not directly readable or writable. As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.
For a GOTO instruction, the PC<8:0> is provided by the GOTO instruction word. The PC<9> is cleared to “0”. The PCL register is mapped to PC<7:0>.
For a CALL instruction, the PC<7:0> is provided by the CALL instruction word. The PC<9:8> is cleared to “0”. The next PC will be loaded (PUSHed) onto the top of STACK. The PCL register is mapped to PC<7:0>.
For a LGOTO instruction, the PC<9:0> is provided by the LGOTO instruction word. The PCL register is mapped to PC<7:0>.
For a LCALL instruction, the PC<9:0> is provided by the LCALL instruction word. The next PC will be loaded (PUSHed) onto the top of STACK. The PCL register is mapped to PC<7:0>.
For a RETIA, or RETURN instruction, the PC are updated (POPed) from the top of STACK. The PCL register is mapped to PC<7:0>.
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result. However, the PC<9:8> will be cleared to “0”.

FIGURE 2.2: Loading of PC in Different Situations

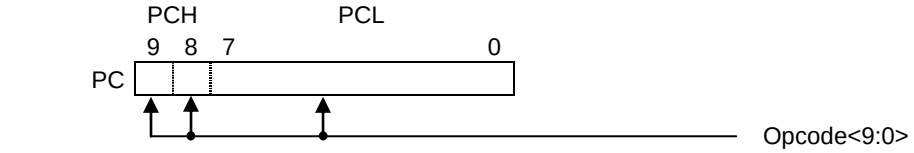
Situation 1: **GOTO** Instruction



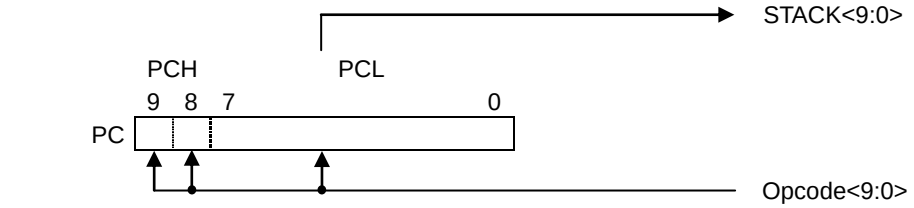
Situation 2: **CALL** Instruction



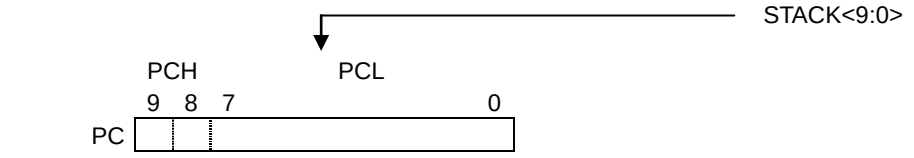
Situation 3: **LGOTO** Instruction



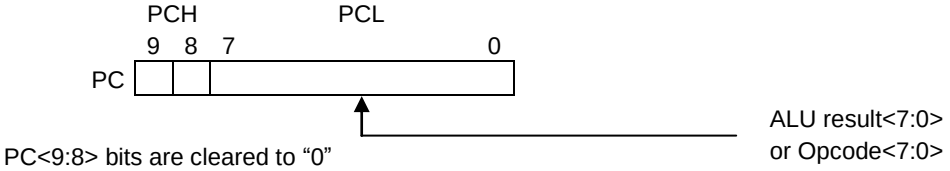
Situation 4: **LCALL** Instruction



Situation 5: **RETIA**, or **RETURN** Instruction



Situation 6: Instruction with PCL as destination



2.1.4 STATUS (Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
03h (r/w)	STATUS	GP2	GP1	GP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

This register contains the arithmetic status of the ALU, the RESET status.
If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C : Carry/borrow bit.
ADDAR, ADDIA
= 1, a carry occurred.
= 0, a carry did not occur.
SUBAR, SUBIA
= 1, a borrow did not occur.
= 0, a borrow occurred.
Note : A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC : Half carry/half borrow bit.
ADDAR, ADDIA
= 1, a carry from the 4th low order bit of the result occurred.
= 0, a carry from the 4th low order bit of the result did not occur.
SUBAR, SUBIA
= 1, a borrow from the 4th low order bit of the result did not occur.
= 0, a borrow from the 4th low order bit of the result occurred.

Z : Zero bit.
= 1, the result of a logic operation is zero.
= 0, the result of a logic operation is not zero.

$\overline{PD}$: Power down flag bit.
= 1, after power-up or by the CLRWDT instruction.
= 0, by the SLEEP instruction.

$\overline{TO}$: Time overflow flag bit.
= 1, after power-up or by the CLRWDT or SLEEP instruction.
= 0, a watch-dog time overflow occurred.

GP2:GP0 : General purpose read/write bits.

2.1.5 FSR (Indirect Data Memory Address Pointer)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
04h (r/w)	FSR	*	RP0	Indirect data memory address pointer					

Bit5:Bit0 : Select registers address in the indirect addressing mode. See 2.1.1 for detail description.

RP0 : This bit is used to switching the bank of two data memory banks. See 2.1.1 for detail description.

Bit7 : Not used. Read as “1”.

2.1.6 PORTA, PORTB & PORTC (Port Data Registers)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
05h (r/w)	PORTA	IOA7	IOA6	IOA5	IOA4	IOA3	IOA2	IOA1	IOA0
06h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
07h (r/w)	PORTC	-	-	-	-	IOC3	IOC2	IOC1	IOC0

Both PORTA and PORTB are 8-bit port data registers. Reading the port (PORTA, PORTB register) reads the status of the pins independent of the pin’s input/output modes.
PORTC is a 4-bit port data Register. Only the low order 4 bits are used (PORTC<3:0>). Bits 7-4 are unimplemented and read as ‘0’s. And IOC1 is an input pin only.
Writing to these ports will write to the port data latch.

2.1.7 ACC (Accumulator)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (r/w)	ACC	Accumulator							

Accumulator is an internal data transfer, or instruction operand holding. It can not be addressed.

2.1.8 OPTION Register

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (w)	OPTION	-	T0CS1	T0CS0	T0SE	PSA	PS2	PS1	PS0

Accessed by OPTION instruction.

By executing the OPTION instruction, the contents of the ACC Register will be transferred to the OPTION Register. The OPTION Register is a 7-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler, and Timer0.
The OPTION Register are “write-only” and are set all “1.

PS2:PS0 : Prescaler rate select bits.

PS2:PS0	Timer0 Rate	WDT Rate
0 0 0	1:2	1:1
0 0 1	1:4	1:2
0 1 0	1:8	1:4
0 1 1	1:16	1:8
1 0 0	1:32	1:16
1 0 1	1:64	1:32
1 1 0	1:128	1:64
1 1 1	1:256	1:128

PSA : Prescaler assign bit.
= 1, WDT (watch-dog timer).
= 0, TMR0 (Timer0).

T0SE : TMR0 source edge select bit.
= 1, Falling edge on T0CKI pin.
= 0, Rising edge on T0CKI pin.

T0CS1:T0CS0 : TMR0 clock source select bit.
= 1, 1 → External T0CKI pin.
= 1, 0 → Internal instruction clock cycle.
= 0, X → Internal IROUT clock source.

Bit7 : Not used.

2.1.9 IOSTA, IOSTB & IOSTC (Port I/O Control Registers)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
05h (w)	IOSTA	Port A I/O Control Register							
06h (w)	IOSTB	Port B I/O Control Register							
07h (w)	IOSTC	-	-	-	-	Port C I/O Control Register			

Accessed by IOST instruction.

The Port I/O Control Registers are loaded with the contents of the ACC Register by executing the IOST R (05h~07h) instruction. A '1' from a IOST Register bit puts the corresponding output driver in hi-impedance state (input mode). A '0' enables the output buffer and puts the contents of the output data latch on the selected pins (output mode). The IOST Registers are "write-only" and are set (output drivers disabled) upon RESET.

2.1.10 CMPCON (Comparator Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
08h (r/w)	CMPCON	GP3	CMPON	VREF1	VREF0	C3ON	C2ON	C1ON	C0ON

Accessed by IOST instruction.

C0ON : = 0, IOA0 pin is selected of IOA0/CMP0 pin
= 1, CMP0 pin is selected of IOA0/CMP0 pin

C1ON : = 0, IOA1 pin is selected of IOA1/CMP1 pin
= 1, CMP1 pin is selected of IOA1/CMP1 pin

C2ON : = 0, IOA2 pin is selected of IOA2/CMP2 pin
= 1, CMP2 pin is selected of IOA2/CMP2 pin

C3ON : = 0, IOA3 pin is selected of IOA3/CMP3 pin
= 1, CMP3 pin is selected of IOA3/CMP3 pin

VREF1:VREF0 : Comparator reference voltage select bits
= 0, 0 → 1/4 Vdd
= 0, 1 → 2/4 Vdd
= 1, 0 → 3/4 Vdd
= 1, 1 → VREF pin (IOA4/VREF pin must be set to input)

CMPON : Comparator module enable bit.
= 1, Enable the comparator module.
= 0, Disable the comparator module.

GP3 : General purpose read/write bits.

2.1.11 PCON (Power Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
09h (w)	PCON	WDTE	-	LVDTE	-	-	IROEN	IRSC	IREN

Accessed by IOST instruction.

WDTE : WDT (watch-dog timer) enable bit.
= 0, Disable WDT.
= 1, Enable WDT.

LVDTE : LVDT (low voltage detector) enable bit.
= 0, Disable LVDT.
= 1, Enable LVDT.

IROEN :IROUT output enable bit.
= 0, IROUT is disabled.
= 1, IROUT is enabled.

IRSC : IROUT pin drive/sink current select bit.
= 0, Normal.
= 1, Heavy.

IREN : IOB0/IROUT pin select bit.
= 0, IOB0 is selected and IR module is disabled.
= 1, IROUT is selected and IR module is enabled.

2.1.12 AWUCON (Port A Input Change Wake-up Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ah (w)	AWUCON	WUA7	WUA6	WUA5	WUA4	WUA3	WUA2	WUA1	WUA0

Accessed by IOST instruction.

WUA0 : = 1, Enable the input falling wake-up function of IOA0 pin.
= 0, Disable the input falling wake-up function of IOA0 pin.

WUA1 : = 1, Enable the input falling wake-up function of IOA1 pin.
= 0, Disable the input falling wake-up function of IOA1 pin.

WUA2 : = 1, Enable the input falling wake-up function of IOA2 pin.
= 0, Disable the input falling wake-up function of IOA2 pin.

WUA3 : = 1, Enable the input falling wake-up function of IOA3 pin.
= 0, Disable the input falling wake-up function of IOA3 pin.

WUA4 : = 1, Enable the input falling wake-up function of IOA4 pin.
= 0, Disable the input falling wake-up function of IOA4 pin.

WUA5 : = 1, Enable the input falling wake-up function of IOA5 pin.
= 0, Disable the input falling wake-up function of IOA5 pin.

WUA6 : = 1, Enable the input falling wake-up function of IOA6 pin.
= 0, Disable the input falling wake-up function of IOA6 pin.

WUA7 : = 1, Enable the input falling wake-up function of IOA7 pin.
= 0, Disable the input falling wake-up function of IOA7 pin.

2.1.13 BWUCON (Port B Input Change Wake-up Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Bh (w)	BWUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

Accessed by IOST instruction.

WUB0 : = 1, Enable the input falling wake-up function of IOB0 pin.
= 0, Disable the input falling wake-up function of IOB0 pin.

WUB1 : = 1, Enable the input falling wake-up function of IOB1 pin.
= 0, Disable the input falling wake-up function of IOB1 pin.

WUB2 : = 1, Enable the input falling wake-up function of IOB2 pin.
= 0, Disable the input falling wake-up function of IOB2 pin.

WUB3 : = 1, Enable the input falling wake-up function of IOB3 pin.
= 0, Disable the input falling wake-up function of IOB3 pin.

WUB4 : = 1, Enable the input falling wake-up function of IOB4 pin.
= 0, Disable the input falling wake-up function of IOB4 pin.

WUB5 : = 1, Enable the input falling wake-up function of IOB5 pin.
= 0, Disable the input falling wake-up function of IOB5 pin.

WUB6 : = 1, Enable the input falling wake-up function of IOB6 pin.
= 0, Disable the input falling wake-up function of IOB6 pin.

WUB7 : = 1, Enable the input falling wake-up function of IOB7 pin.
= 0, Disable the input falling wake-up function of IOB7 pin.

2.1.14 CWUCON (Port C Input Change Wake-up Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ch (w)	CWUCON	-	-	-	-	WUC3	WUC2	WUC1	WUC0

Accessed by IOST instruction.

WUC0 : = 1, Enable the input falling wake-up function of IOC0 pin.
= 0, Disable the input falling wake-up function of IOC0 pin.

WUC1 : = 1, Enable the input falling wake-up function of IOC1 pin.
= 0, Disable the input falling wake-up function of IOC1 pin.

WUC2 : = 1, Enable the input falling wake-up function of IOC2 pin.
= 0, Disable the input falling wake-up function of IOC2 pin.

WUC3 : = 1, Enable the input falling wake-up function of IOC3 pin.
= 0, Disable the input falling wake-up function of IOC3 pin.

2.1.15 IRCYCLE (IROUT Cycle Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Dh (w)	IRCYCLE	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0

Accessed by IOST instruction.

IRC7:IRC0 : IROUT (IR Carrier output) frequency = (Oscillator frequency) / (IRC7:IRC0).

2.1.16 IRDUTY (IROUT Duty Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Eh (w)	IRDUTY	IRD7	IRD6	IRD5	IRD4	IRD3	IRD2	IRD1	IRD0

Accessed by IOST instruction.

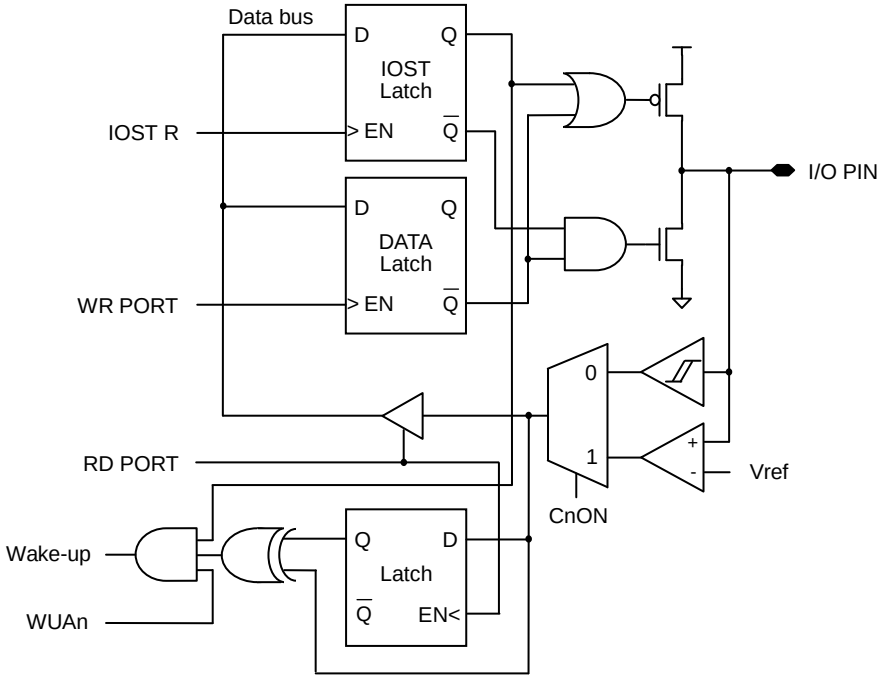
IRD7:IRD0 : IROUT (IR Carrier output) duty cycle = (IRD7:IRD0) / (IRC7:IRC0).
(IRD7:IRD0) must be less than (IRC7:IRC0).

2.2 I/O Ports

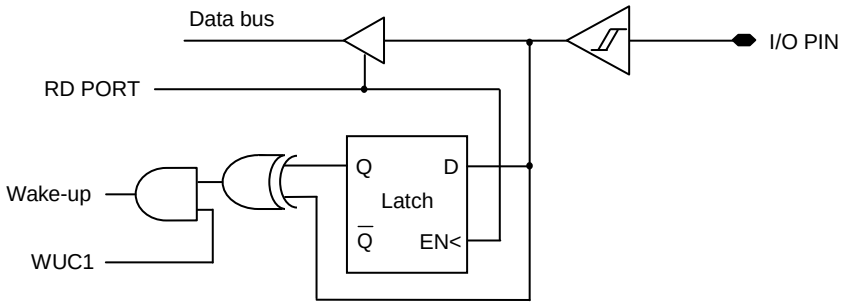
Port A , port B, and port C are bi-directional tri-state I/O ports. Both Port A and Port B are 8-pin I/O ports. Port C is a 4-pin I/O port. Please note that IOC1 is an input pin only.
All I/O pins (IOA<7:0>, IOB<7:0>, and IOC<3:0>) have data direction control registers (IOSTA, IOSTB, and IOSTC) which can configure these pins as output or input. The exception is IOC1 which is input only.
All of IOA<7:0>, IOB<7:0>, and IOC<3:0> also provide the input change wake-up function. Each pin has its corresponding input change wake-up enable bits (AWUCON, BWUCON, & CWUCON registers) to select the input change wake-up source.
The CONFIGURATION words can set several I/Os to alternate functions. When acting as alternate functions the pins will read as “0” during port read.

FIGURE 2.3: Block Diagram of I/O PINs

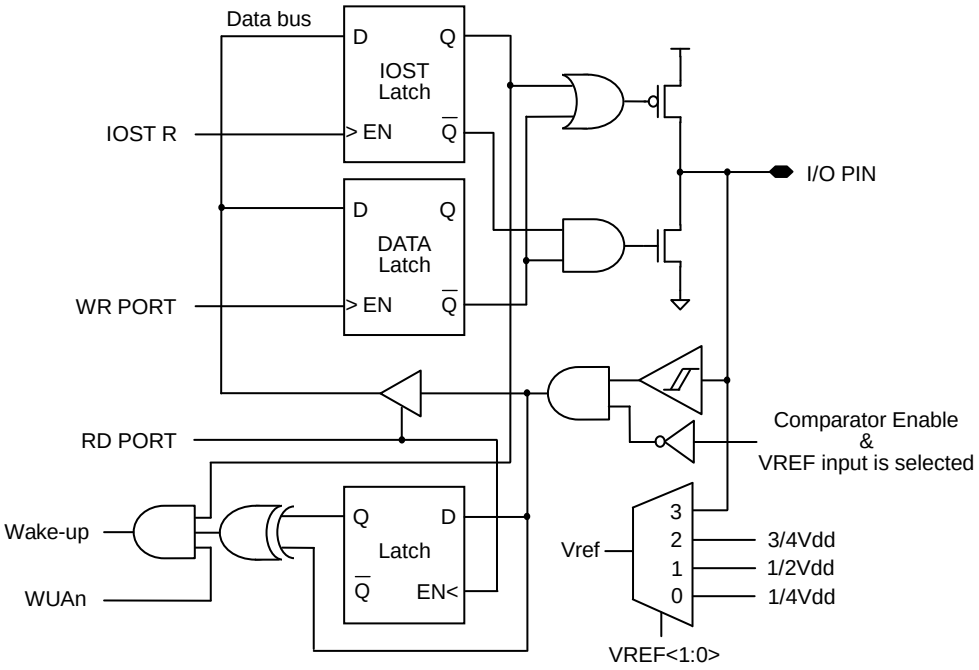
IOA3 ~ IOA0 :



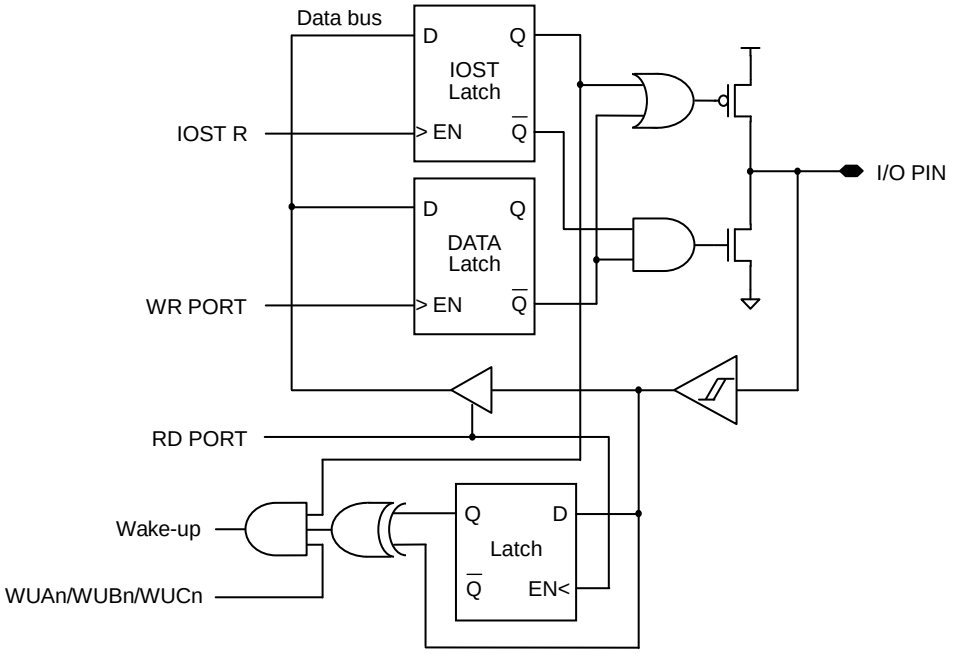
IOC1 :



IOA4 :



IOA5 ~ IOA7, IOB0 ~ IOB7, IOC3, IOC2 & IOC0 :



2.3 Timer0/WDT & Prescler

2.3.1 Timer0

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the internal clock, an external clock source (T0CKI pin), or by an internal IROUT clock source.

2.3.1.1 Using Timer0 with an Internal Clock : Timer mode

Timer mode is selected by clearing the T0CS0 bit (OPTION<5>) and setting the T0CS1 bit (OPTON<6>). In timer mode, the timer0 register (TMR0) will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles.

2.3.1.2 Using Timer0 with an External Clock : Counter1 mode

Counter1 mode is selected by setting the T0CS0 bit (OPTON<5>) and the T0CS1 bit (OPTON<6>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>).
The external clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the T2 and T4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 T_{OSC} and low for at least 2 Tosc.
When a prescaler is used, the external clock input is divided by the asynchronous prescaler. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc divided by the prescaler value.

2.3.1.3 Using Timer0 with an IROUT Clock : Counter2 mode

Counter2 mode is selected by clearing the T0CS1 bit (OPTON<6>). In this mode, Timer0 will increment either on every rising or falling edge of internal IROUT clock source. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>).
The IROUT clock requirement is due to internal phase clock (Tosc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.
When no prescaler is used, the IROUT clock input is the same as the prescaler output. The synchronization of IROUT clock with the internal phase clocks is accomplished by sampling the prescaler output on the T2 and T4 cycles of the internal phase clocks. Therefore, it is necessary for IROUT clock to be high for at least 2 T_{OSC} and low for at least 2 Tosc.
When a prescaler is used, the IROUT clock input is divided by the asynchronous prescaler. For the IROUT clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for IROUT clock to have a period of at least 4Tosc divided by the prescaler value.

2.3.2 Watchdog Timer (WDT)

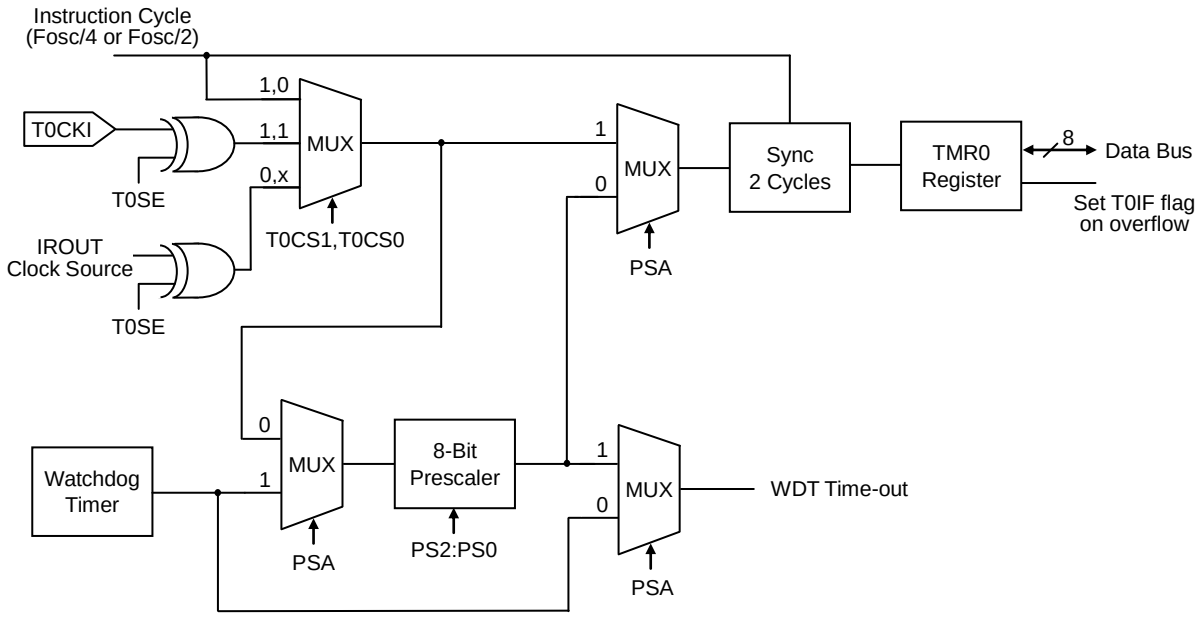
The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. So the WDT will still run even if the clock on the OSCI and OSCO pins is turned off, such as in SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset and the $\overline{TO}$ bit (STATUS<4>) will be cleared.
The WDT can be disabled by clearing the control bit WDTE (PCON<7>) to “0”.
The WDT has a nominal time-out period of 18 ms (without prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT controlled by the OPTION register. Thus, the longest time-out period is approxmately 2.3 seconds.
The CLRWDT instruction clears the WDT and the prescaler, if assigned to the WDT, and prevents it from timing out and generating a device reset.

The SLEEP instruction resets the WDT and the prescaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

2.3.3 Prescaler

An 8-bit counter (down counter) is available as a prescaler for the Timer0, or as a postscaler for the Watchdog Timer (WDT). Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 means that there is no prescaler for the WDT, and vice-versa.
The PSA bit (OPTION<3>) determines prescaler assignment. The PS<2:0> bits (OPTION<2:0>) determine prescaler ratio.
When the prescaler is assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the prescaler. When it is assigned to WDT, a CLRWDT instruction will clear the prescaler along with the WDT.
The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '1's.
To avoid an unintended device reset, CLRWDT or CLRR TMR0 instructions must be executed when changing the prescaler assignment from Timer0 to the WDT, and vice-versa.

FIGURE 2.4: Block Diagram of The Timer0/WDT Prescaler



2.4 IR Carrier Output (IROUT)

AT8A22 is build-in an IR carrier output generator. The output is controlled by IROEN (PCON<2>), IRSC (PCON<1>), IREN (PCON<0>) bits and IRCYCLE, IRDUTY registers.
The IROUT frequency and duty cycle are following the equations below:

IROUT frequency = (Oscillator frequency) / IRCYCLE<7:0>
IROUT duty cycle = IRDUTY<7:0> / IRCYCLE<7:0>

For example, if oscillator frequency is equal to 455KHz, and the IRCYCLE = 12, and IRDUTY = 6, then
IROUT frequency = 455KHz / 12 = 38KHz, and
IROUT duty cycle = 6 / 12 = 50%

Note: before enabling the IROUT (set IREN = "1"), set the IOB0 pin to be an output pin and output "high" for negative pulse or "low" for positive pulse is needed.
The value of IRDUTY<7:0> must be less than IRCYCLE<7:0>.

FIGURE 2.5: IROUT Waveform with Negative Pulse

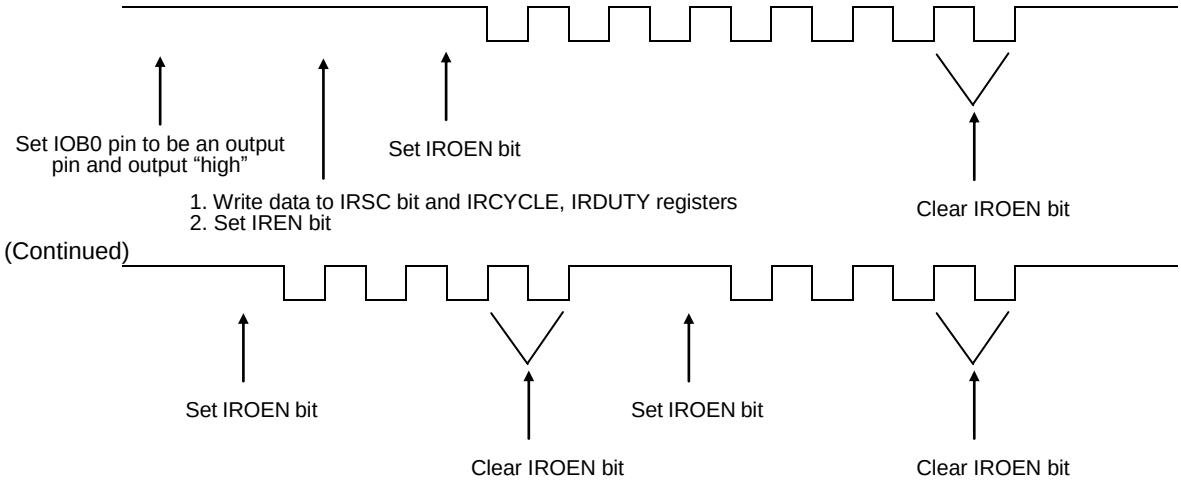
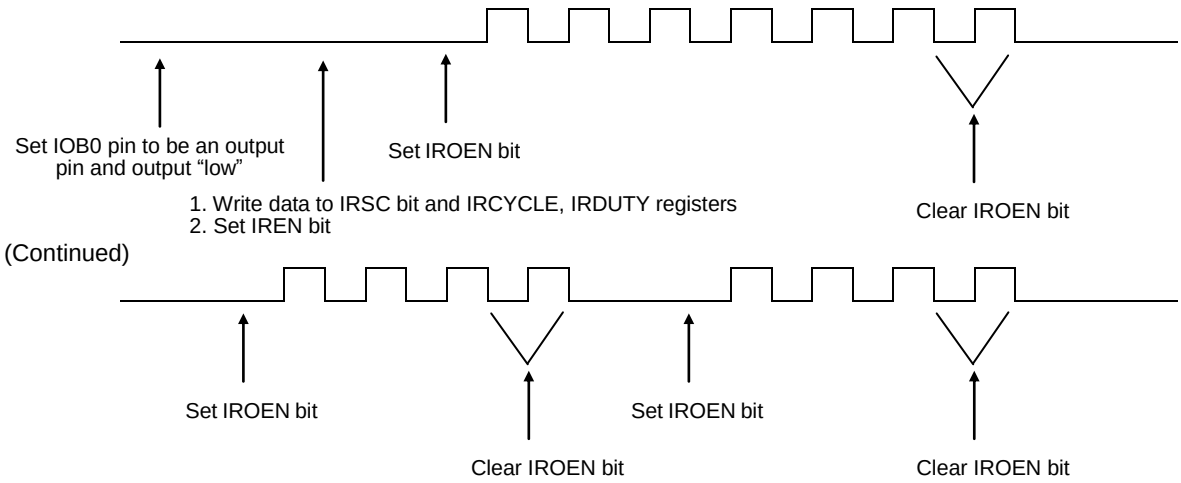


FIGURE 2.6: IROUT Waveform with Positive Pulse



2.5 Comparator Module

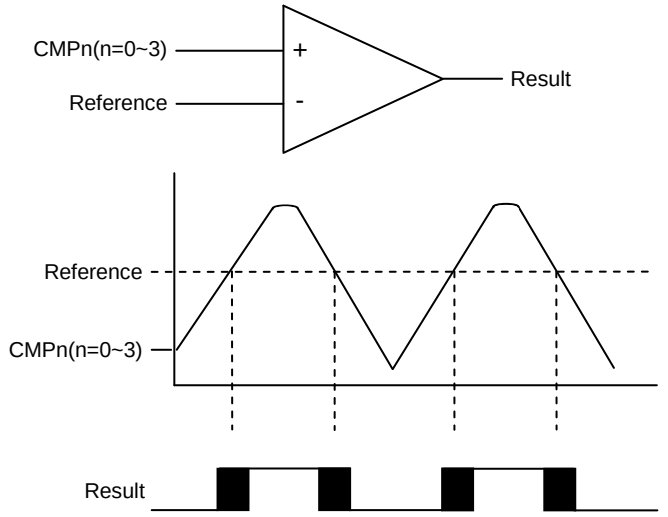
The Comparator module contains four analog comparators. The inputs to the comparator are multiplexed with IOA0 ~ IOA3 pins.
The CMPCON register controls the comparator operation. If CnON (n=0~3) = 0 means the general purpose I/O function is selected of the IOAn/CMPn (n=0~3) pin; or if CnON (n=0~3) = 1 means the comparator function is selected of the IOAn/CMPn (n=0~3) pin.
Four internal reference signal and one external reference signal input may be used selected by depending on the comparator reference control bits (VREF<1:0>).

TABLE 2.1: Comparator Reference Selecion

VREF1:VREF0	Comparator reference
0, 0	1/4 Vdd
0, 1	2/4 Vdd
1, 0	3/4 Vdd
1, 1	VREF pin (IOA4/VREF pin must be set to input)

When the analog input at CMPn (n=0~3) is less than the reference voltage, the output of the comparator is a digital low level. When the analog input at CMPn (n=0~3) is greater than the reference voltage, the output of the comparator is a digital high level.
The analog inputs and reference input voltage range is 0V ~ (VDD-0.8V).
The comparator output is read through IOA<3:0> bits (PORTA<3:0>).

FIGURE 2.7: SINGLE COMPARATOR



2.5.1 Comparator Operation During Sleep

When the comparator is active in Sleep mode, the comparator remains active. And higher Sleep currents than shown in the power-down current specification will occur. The device can wake-up from SLEEP mode through the output of the comparator has changed state if enabled. To minimize power consumption while in Sleep mode, turn off the comparator (by clear the CMPON bit) before entering Sleep.

2.6 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.
When SLEEP instruction is executed, the $\overline{PD}$ bit (STATUS<3>) is cleared, the $\overline{TO}$ bit is set, the watchdog timer will be cleared and keeps running, and the oscillator driver is turned off.
All I/O pins maintain the status they had before the SLEEP instruction was executed.
To save the power consumption, if the low voltage detector (LVDT) is enabled, user can disable the LVDT by clearing the control bit LVDTE (PCON<5>) before entering into SLEEP mode.

2.6.1 Wake-up from SLEEP Mode

The device can wake-up from SLEEP mode through one of the following events:
1. RSTB reset.
2. WDT time-out reset (if enabled).
3. PORTA and/or PORTB input status change.

External RSTB reset and WDT time-out reset will cause a device reset. The $\overline{PD}$ and $\overline{TO}$ bits can be used to determine the cause of device reset. The $\overline{PD}$ bit is set on power-up and is cleared when SLEEP instruction is executed. The $\overline{TO}$ bit is cleared if a WDT time-out occurred.
For the device to wake-up through a PORTA/PORTB input status changing event, and the program will execute next PC after wake-up. Before entering SLEEP mode, reading PORTA/PORTB (any instruction accessed to PORTA/PORTB, including read/write instructions) is necessary. Any pin which corresponding WUAn/WUBn bit (AWUCON<7:0> / BWUCON<7:0>) is cleared to “0” or configured as output will be excluded from this function.
The system wake-up delay time is 18ms/140us/36ms/72ms (selected by SUT<1:0> bits of configuration word) plus 128 oscillator cycles time.

TABLE 2.2: System Wake-up Delay Time

Oscillator Mode	Wake-up Delay Time
ERC & IRC & ERIC	140us/18ms/36ms/72ms
HF & XT & LF	18ms/36ms/72ms

2.7 Reset

AT8A22 devices may be RESET in one of the following ways:
1. Power-on Reset (POR)
2. Brown-out Reset (BOR)
3. RSTB Pin Reset
4. WDT time-out Reset

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a “reset state” on Power-on Reset, RSTB or WDT Reset.
A Power-on RESET pulse is generated on-chip when Vdd rise is detected. To use this feature, the user merely ties the RSTB pin to Vdd.
On-chip Low Voltage Detector (LVD) places the device into reset when Vdd is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation Vdd range. Brown-out RESET is typically used in AC line or heavy loads switched applications.
A RSTB or WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.
The $\overline{TO}$ and $\overline{PD}$ bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

2.7.1 Power-up Reset Timer(PWRT)

The Power-up Reset Timer provides a nominal 18ms/140us/36ms/72ms (selected by SUT<1:0> bits of configuration word and reset condition) delay after Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or

WDT time-out Reset. The device is kept in reset state as long as the PWRT is active.
The PWDT delay will vary from device to device due to Vdd, temperature, and process variation.

TABLE 2.3: PWRT Period

Oscillator Mode	Power-on Reset Brown-out Reset	RSTB Reset WDT time-out Reset
ERC & IRC & ERIC	18ms/36ms/72ms	140us/18ms/36ms/72ms
HF & XT & LF	18ms/36ms/72ms	18ms/36ms/72ms

2.7.2 Oscillator Start-up Timer(OST)

The OST timer provides a 128 oscillator cycles delay (from OSCI input) after the PWRT delay (140us/18ms/36ms/72ms) is over. This delay ensures that the X'tal oscillator or resonator has started and stabilized. The device is kept in reset state as long as the OST is active.
This counter only starts incrementing after the amplitude of the OSCI signal reaches the oscillator input thresholds.

2.7.3 Reset Sequence

When Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset is detected, the reset sequence is as follows:

1. The reset latch is set and the PWRT & OST are cleared.
2. When the internal POR, BOR, RSTB Reset or WDT time-out Reset pulse is finished, then the PWRT begins counting.
3. After the PWRT time-out, the OST is activated.
4. And after the OST delay is over, the reset latch will be cleared and thus end the on-chip reset signal.

The totally system reset delay time is 18ms/140us/36ms/72ms plus 128 oscillator cycle time.

FIGURE 2.8: Simplified Block Diagram of on-chip Reset Circuit

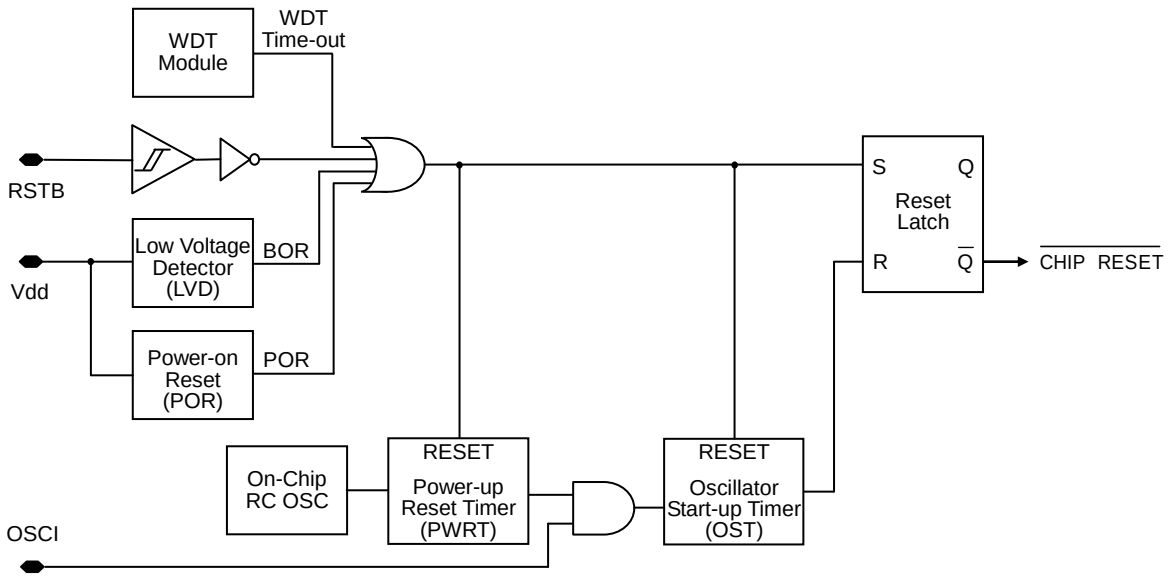


TABLE 2.4: Reset Conditions for All Registers

Register	Address	Power-on Reset Brown-out Reset	RSTB Reset WDT Reset
ACC	N/A	xxxx xxxx	uuuu uuuu
OPTION	N/A	-111 1111	-111 1111
IOSTA	05h	1111 1111	1111 1111
IOSTB	06h	1111 1111	1111 1111
IOSTC	07h	---- 11-1	---- 11-1
CMPCON	08h	0000 0000	0000 0000
CWUCON	09h	---- 0000	---- 0000
PCON	0Ah	1-1- -000	1-1- -000
AWUCON	0Bh	0000 0000	0000 0000
BWUCON	0Ch	0000 0000	0000 0000
IRCYCLE	0Dh	0000 1100	0000 1100
IRDUTY	0Eh	0000 0110	0000 0110
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
FSR	04h	11xx xxxx	11uu uuuu
PORTA	05h	xxxx xxxx	uuuu uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC	07h	---- xxxx	---- uuuu
General Purpose Registers	08 ~ 3Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented,
= refer to the following table for possible values.

TABLE 2.5: $\overline{TO}$ / $\overline{PD}$ Status after Reset

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-on Reset
1	1	Brown-out reset
u	u	RSTB Reset during normal operation
1	0	RSTB Reset during SLEEP
0	1	WDT Reset during normal operation
0	0	WDT Reset during SLEEP

Legend: u = unchanged

TABLE 2.6: Events Affecting $\overline{TO}$ / $\overline{PD}$ Status Bits

Event	$\overline{TO}$	$\overline{PD}$
Power-on	1	1
WDT Time-Out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Legend: u = unchanged

2.8 Oscillator Configurations

AT8A22 can be operated in six different oscillator modes. Users can program three configuration bits (Fosc<2:0>) to select the appropriate modes:

- ERC: External Resistor/Capacitor Oscillator
- HF: High Frequency Crystal/Resonator Oscillator
- XT: Crystal/Resonator Oscillator
- LF: Low Frequency Crystal Oscillator
- IRC: Internal Resistor/Capacitor Oscillator (455KHz)
- ERIC: External Resistor/ Internal Capacitor Oscillator

In LF, XT, or HF modes, a crystal or ceramic resonator in connected to the OSCI and OSCO pins to establish oscillation. When in LF, XT, or HF modes, the devices can have an external clock source drive the OSCI pin. The RC (including ERC, ERIC, and IRC modes) device option offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the supply voltage, the resistor (Rext or Rint) and capacitor (Cext or Cint), the operating temperature, and the process parameter.

FIGURE 2.9: HF, XT or LF Oscillator Modes (Crystal Operation or Ceramic Resonator)

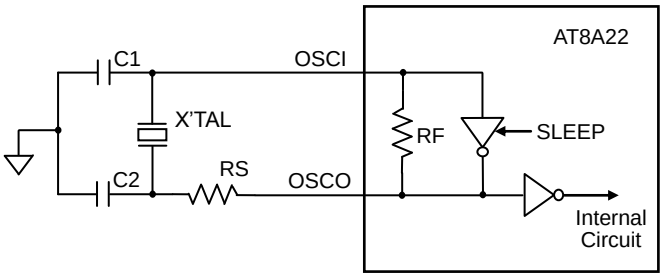


FIGURE 2.10: HF, XT or LF Oscillator Modes (External Clock Input Operation)

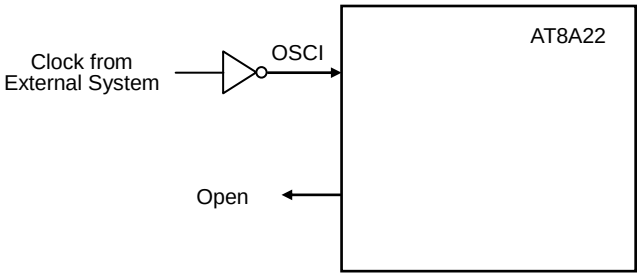


FIGURE 2.11: ERC Oscillator Mode

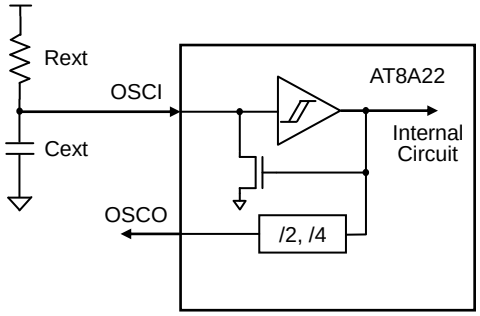


FIGURE 2.12: ERIC Oscillator Mode

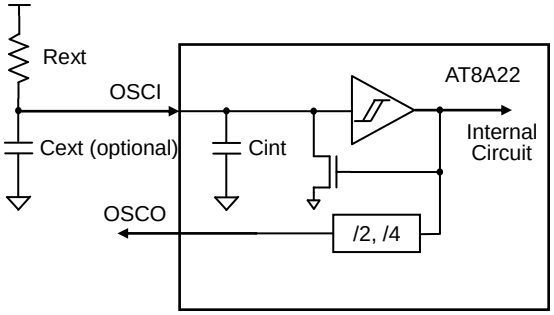
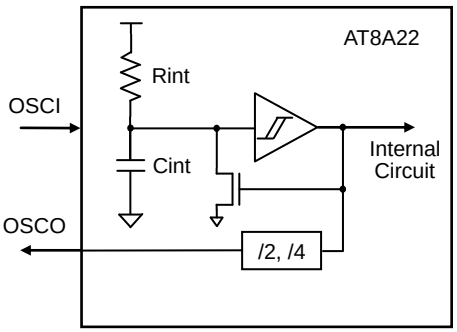


FIGURE 2.13: IRC Oscillator Mode (Internal R, Internal C Oscillator)



2.9 Configurations Words

TABLE 2.7: Configurations Word 0

Name	Description
Fosc<2:0>	Oscillator Selection Bits = 1, 1, 1 → ERC mode (external R & C) (default) = 1, 1, 0 → HF mode = 1, 0, 1 → XT mode = 1, 0, 0 → LF mode = 0, 1, 1 → IRC mode (internal R & C) = 0, 1, 0 → ERIC mode (external R & internal C)
LVDTEN	Low Voltage Detector Enable Bit = 1, disable (default) = 0, enable, LVDT voltage = 1.8V
SUT<1:0>	Reset Delay Time Selection Bits = 1, 1 → 18 ms (default) = 1, 0 → 140 us = 0, 1 → 36 ms = 0, 0 → 72 ms
PAPH	Port A internal pull-high Enable Bit = 1, Disable (default) = 0, Enable
PBPH	Port B internal pull-high Enable Bit = 1, Disable (default) = 0, Enable
PCPH	Port C internal pull-high Enable Bit = 1, Disable (default) = 0, Enable
OSCOUT	IOC2/OSCO Pin Selection Bit for ERC/IRC/ERIC Mode = 1, OSCO pin is selected (default) = 0, IOC2 pin is selected
RSTBIN	IOC1/RSTB Pin Selection Bit = 1, IOC1 pin is selected (default) = 0, RSTB pin is selected
-	Unused

TABLE 2.8: Configurations Word 1

Name	Description
CAL<6:0>	Calibration Selection Bits for IRC Mode
WDTEN	Watchdog Timer Enable Bit = 1, WDT enabled (default) = 0, WDT disabled
PROTECT	Code Protection Bit = 1, EPROM code protection off (default) = 0, EPROM code protection on
OSCD	Instruction Period Selection Bits = 1, four oscillator periods (default) = 0, two oscillator periods
PMOD	Power Mode Selection Bit = 1, Non-power saving (default) = 0, Power saving
-	Unused

TABLE 2.9: Selection of IOC3/OSCI and IOC2/OSCO Pins

Mode of oscillation	IOC3/OSCI	IOC2/OSCO
IRC	IOC3	IOC2/OSCO selected by OSCOUT bit
ERC, ERIC	OSCI	IOC2/OSCO selected by OSCOUT bit
HF, XT, LF	OSCI	OSCO

3.0 INSTRUCTION SET

Mnemonic, Operands		Description	Operation	Cycles	Status Affected
BCR	**R, bit**	Clear bit in R	0 → R<b>	1	-
BSR	**R, bit**	Set bit in R	1 → R<b>	1	-
BTRSC	**R, bit**	Test bit in R, Skip if Clear	Skip if R<b> = 0	1/2	-
BTRSS	**R, bit**	Test bit in R, Skip if Set	Skip if R<b> = 1	1/2	-
NOP		No Operation	No operation	1	-
CLRWDT		Clear Watchdog Timer	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
OPTION		Load OPTION register	ACC → OPTION	1	-
SLEEP		Go into power-down mode	00h → WDT, 00h → WDT prescaler	1	$\overline{TO}$, $\overline{PD}$
IOST	**R**	Load IOST register	ACC → IOST register	1	-
RETURN		Return from subroutine	Top of Stack → PC	2	-
CLRA		Clear ACC	00h → ACC	1	Z
CLRR	**R**	Clear R	00h → R	1	Z
MOVAR	**R**	Move ACC to R	ACC → R	1	-
MOVR	**R, d**	Move R	R → dest	1	Z
DECR	**R, d**	Decrement R	R - 1 → dest	1	Z
DECRSZ	**R, d**	Decrement R, Skip if 0	R - 1 → dest, Skip if result = 0	1/2	-
INCR	**R, d**	Increment R	R + 1 → dest	1	Z
INCRSZ	**R, d**	Increment R, Skip if 0	R + 1 → dest, Skip if result = 0	1/2	-
ADDAR	**R, d**	Add ACC and R	R + ACC → dest	1	C, DC, Z
SUBAR	**R, d**	Subtract ACC from R	R - ACC → dest	1	C, DC, Z
ANDAR	**R, d**	AND ACC with R	ACC and R → dest	1	Z
IORAR	**R, d**	Inclusive OR ACC with R	ACC or R → dest	1	Z
XORAR	**R, d**	Exclusive OR ACC with R	R xor ACC → dest	1	Z
COMR	**R, d**	Complement R	$\overline{R}$ → dest	1	Z
RLR	**R, d**	Rotate left R through Carry	R<7> → C, R<6:0> → dest<7:1>, C → dest<0>	1	C
RRR	**R, d**	Rotate right R through Carry	C → dest<7>, R<7:1> → dest<6:0>, R<0> → C	1	C
SWAPR	**R, d**	Swap R	R<3:0> → dest<7:4>, R<7:4> → dest<3:0>	1	-
MOVIA	**I**	Move Immediate to ACC	I → ACC	1	-
ADDIA	**I**	Add ACC and Immediate	I + ACC → ACC	1	C, DC, Z
SUBIA	**I**	Subtract ACC from Immediate	I - ACC → ACC	1	C, DC, Z
ANDIA	**I**	AND Immediate with ACC	ACC and I → ACC	1	Z
IORIA	**I**	OR Immediate with ACC	ACC or I → ACC	1	Z
XORIA	**I**	Exclusive OR Immediate to ACC	ACC xor I → ACC	1	Z

RETIA	**I**	Return, place Immediate in ACC	I → ACC, Top of Stack → PC	2	-
CALL	**I**	Call subroutine	PC + 1 → Top of Stack, I → PC<7:0>, 0 → PC<9:8>	2	-
GOTO	**I**	Unconditional branch	I → PC<8:0>, 0 → PC<9>	2	-
LCALL	**I**	Call subroutine	PC + 1 → Top of Stack, I → PC<9:0>	2	-
LGOTO	**I**	Unconditional branch	I → PC<9:0>	2	-

Note: bit : Bit address within an 8-bit register R
R : Register address (00h to 3Fh)
I : Immediate data
ACC : Accumulator
d : Destination select;
=0 (store result in ACC)
=1 (store result in file register R)
dest : Destination
PC : Program Counter
WDT : Watchdog Timer Counter
GIE : Global interrupt enable bit
$\overline{TO}$: Time-out bit
$\overline{PD}$: Power-down bit
C : Carry bit
DC : Digital carry bit
Z : Zero bit

ADDAR	**Add ACC and R**
Syntax:	ADDAR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	ACC + R → dest
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register and register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ADDIA	**Add ACC and Immediate**
Syntax:	ADDIA I
Operands:	$0 \leq I \leq 255$
Operation:	ACC + I → ACC
Status Affected:	C, DC, Z
Description:	Add the contents of the ACC register with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

ANDAR	**AND ACC and R**
Syntax:	ANDAR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	ACC and R → dest
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is '1' the result is stored back in register 'R'.
Cycles:	1

ANDIA	**AND Immediate with ACC**
Syntax:	ANDIA I
Operands:	$0 \leq I \leq 255$
Operation:	ACC AND I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are AND'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

BCR	**Clear Bit in R**
Syntax:	BCF R, b
Operands:	$0 \leq R \leq 63$ $0 \leq b \leq 7$
Operation:	0 → R<b>
Status Affected:	None
Description:	Clear bit 'b' in register 'R'.
Cycles:	1

BSR	**Set Bit in R**
Syntax:	BSR R, b
Operands:	$0 \leq R \leq 63$ $0 \leq b \leq 7$
Operation:	1 → R<b>
Status Affected:	None
Description:	Set bit 'b' in register 'R'.
Cycles:	1

BTRSC	**Test Bit in R, Skip if Clear**
Syntax:	BTRSC R, b
Operands:	$0 \leq R \leq 63$ $0 \leq b \leq 7$
Operation:	Skip if R<b> = 0
Status Affected:	None
Description:	If bit 'b' in register 'R' is 0 then the next instruction is skipped. If bit 'b' is 0 then next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead making this a 2-cycle instruction.
Cycles:	1/2

BTRSS	**Test Bit in R, Skip if Set**
Syntax:	BTRSS R, b
Operands:	$0 \leq R \leq 63$ $0 \leq b \leq 7$
Operation:	Skip if R<b> = 1
Status Affected:	None
Description:	If bit 'b' in register 'R' is '1' then the next instruction is skipped. If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.
Cycles:	1/2

CALL	**Subroutine Call**
Syntax:	CALL I
Operands:	$0 \leq I \leq 255$
Operation:	PC +1 → Top of Stack; I → PC<7:0> 0 → PC<9:8>
Status Affected:	None
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The 8-bit immediate address is loaded into PC bits <7:0>. The PC<9:8> is cleared to "0". CALL is a two-cycle instruction.
Cycles:	2

CLRA	**Clear ACC**
Syntax:	CLRA
Operands:	None
Operation:	00h → ACC; 1 → Z
Status Affected:	Z
Description:	The ACC register is cleared. Zero bit (Z) is set.
Cycles:	1

CLRR	**Clear R**
Syntax:	CLRR R
Operands:	$0 \leq R \leq 63$
Operation:	00h → R; 1 → Z
Status Affected:	Z
Description:	The contents of register 'R' are cleared and the Z bit is set.
Cycles:	1

CLRWDT	**Clear Watchdog Timer**
Syntax:	CLRWDT
Operands:	None
Operation:	00h → WDT; 00h → WDT prescaler (if assigned); 1 → $\overline{TO}$; 1 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{TO}$ and $\overline{PD}$ are set.
Cycles:	1

COMR	**Complement R**
Syntax:	COMR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	$\overline{R}$ → dest
Status Affected:	Z
Description:	The contents of register 'R' are complemented. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECR	**Decrement R**
Syntax:	DECR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R - 1 → dest
Status Affected:	Z
Description:	Decrement register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

DECRSZ	**Decrement R, Skip if 0**
Syntax:	DECRSZ R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R - 1 → dest; skip if result =0
Status Affected:	None
Description:	The contents of register 'R' are decremented. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'. If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a 2-cycle instruction.
Cycles:	1/2

GOTO	**Unconditional Branch**
Syntax:	GOTO I
Operands:	$0 \leq I \leq 511$
Operation:	I → PC<8:0> 0 → PC<9>
Status Affected:	None
Description:	GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The PC<9> is cleared to “0”.. GOTO is a two-cycle instruction.
Cycles:	2

INCR	**Increment R**
Syntax:	INCR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R + 1 → dest
Status Affected:	Z
Description:	The contents of register ‘R’ are incremented. If ‘d’ is 0 the result is placed in the ACC register. If ‘d’ is 1 the result is placed back in register ‘R’.
Cycles:	1

INCRSZ	**Increment R, Skip if 0**
Syntax:	INCRSZ R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R + 1 → dest, skip if result = 0
Status Affected:	None
Description:	The contents of register ‘R’ are incremented. If ‘d’ is 0 the result is placed in the ACC register. If ‘d’ is the result is placed back in register ‘R’. If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a 2-cycle instruction.
Cycles:	1/2

IORAR	**OR ACC with R**
Syntax:	IORAR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	ACC or R → dest
Status Affected:	Z
Description:	Inclusive OR the ACC register with register ‘R’. If ‘d’ is 0 the result is placed in the ACC register. If ‘d’ is 1 the result is placed back in register ‘R’.
Cycles:	1

IORIA	**OR Immediate with ACC**
Syntax:	IORIA I
Operands:	$0 \leq I \leq 255$
Operation:	ACC or I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are OR’ed with the 8-bit immediate ‘I’. The result is placed in the ACC register.
Cycles:	1

IOST	**Load IOST Register**
Syntax:	IOST R
Operands:	R = 5 ~ 14
Operation:	ACC → IOST register R
Status Affected:	None
Description:	IOST register 'R' (R = 5 ~ 14) is loaded with the contents of the ACC register.
Cycles:	1

LCALL	**Subroutine Call**
Syntax:	LCALL I
Operands:	$0 \leq I \leq 1023$
Operation:	PC +1 → Top of Stack; I → PC<9:0>
Status Affected:	None
Description:	Subroutine call. First, return address (PC+1) is pushed onto the stack. The 10-bit immediate address is loaded into PC bits <9:0>. LCALL is a two-cycle instruction.
Cycles:	2

LGOTO	**Unconditional Branch**
Syntax:	LGOTO I
Operands:	$0 \leq I \leq 1023$
Operation:	I → PC<9:0>
Status Affected:	None
Description:	LGOTO is an unconditional branch. The 10-bit immediate value is loaded into PC bits <9:0>. LGOTO is a two-cycle instruction.
Cycles:	2

MOVAR	**Move ACC to R**
Syntax:	MOVAR R
Operands:	$0 \leq R \leq 63$
Operation:	ACC → R
Status Affected:	None
Description:	Move data from the ACC register to register 'R'.
Cycles:	1

MOVIA	**Move Immediate to ACC**
Syntax:	MOVIA I
Operands:	$0 \leq I \leq 255$
Operation:	I → ACC
Status Affected:	None
Description:	The 8-bit immediate 'I' is loaded into the ACC register. The don't cares will assemble as 0s.
Cycles:	1

MOVR	**Move R**
Syntax:	MOVR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R → dest
Status Affected:	Z
Description:	The contents of register 'R' is moved to destination 'd'. If 'd' is 0, destination is the ACC register. If 'd' is 1, the destination is file register 'R'. 'd' is 1 is useful to test a file register since status flag Z is affected.
Cycles:	1

NOP	**No Operation**
Syntax:	NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Cycles:	1

OPTION	**Load OPTION Register**
Syntax:	OPTION
Operands:	None
Operation:	ACC → OPTION
Status Affected:	None
Description:	The content of the ACC register is loaded into the OPTION register.
Cycles:	1

RETIA	**Return with Immediate in ACC**
Syntax:	RETIA I
Operands:	$0 \leq I \leq 255$
Operation:	I → ACC; Top of Stack → PC
Status Affected:	None
Description:	The ACC register is loaded with the 8-bit immediate 'I'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RETURN	**Return from Subroutine**
Syntax:	RETURN
Operands:	None
Operation:	Top of Stack → PC
Status Affected:	None
Description:	The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.
Cycles:	2

RLR	**Rotate Left R through Carry**
Syntax:	RLR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R<7> → C; R<6:0> → dest<7:1>; C → dest<0>
Status Affected:	C
Description:	The contents of register 'R' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

RRR	**Rotate RightR through Carry**
Syntax:	RRR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	C → dest<7>; R<7:1> → dest<6:0>; R<0> → C
Status Affected:	C
Description:	The contents of register 'R' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the ACC register. If 'd' is 1 the result is placed back in register 'R'.
Cycles:	1

SLEEP	**Enter SLEEP Mode**
Syntax:	SLEEP
Operands:	None
Operation:	00h → WDT; 00h → WDT prescaler; 1 → $\overline{TO}$; 0 → $\overline{PD}$
Status Affected:	$\overline{TO}$, $\overline{PD}$
Description:	Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared. The processor is put into SLEEP mode.
Cycles:	1

SUBAR	**Subtract ACC from R**
Syntax:	SUBAR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R - ACC → dest
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

SUBIA	**Subtract ACC from Immediate**
Syntax:	SUBIA I
Operands:	$0 \leq I \leq 255$
Operation:	I - ACC → ACC
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) the ACC register from the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

SWAPR	**Swap nibbles in R**
Syntax:	SWAPR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	R<3:0> → dest<7:4>; R<7:4> → dest<3:0>
Status Affected:	None
Description:	The upper and lower nibbles of register 'R' are exchanged. If 'd' is 0 the result is placed in ACC register. If 'd' is 1 the result in placed in register 'R'.
Cycles:	1

XORAR	**Exclusive OR ACC with R**
Syntax:	XORAR R, d
Operands:	$0 \leq R \leq 63$ $d \in [0,1]$
Operation:	ACC xor R → dest
Status Affected:	Z
Description:	Exclusive OR the contents of the ACC register with register 'R'. If 'd' is 0 the result is stored in the ACC register. If 'd' is 1 the result is stored back in register 'R'.
Cycles:	1

XORIA	**Exclusive OR Immediate with ACC**
Syntax:	XORIA I
Operands:	$0 \leq I \leq 255$
Operation:	ACC xor I → ACC
Status Affected:	Z
Description:	The contents of the ACC register are XOR'ed with the 8-bit immediate 'I'. The result is placed in the ACC register.
Cycles:	1

4.0 ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0℃ to +70℃
Store Temperature	-65℃ to +150℃
DC Supply Voltage (Vdd)	0V to +6.0V
Input Voltage with respect to Ground (Vss)	-0.3V to (Vdd + 0.3)V

5.0 OPERATING CONDITIONS

DC Supply Voltage	+2.3V to +5.5V
Operating Temperature	0℃ to +70℃

6.0 ELECTRICAL CHARACTERISTICS

6.1 ELECTRICAL CHARACTERISTICS of AT8A22E

Under Operating Conditions, at four clock instruction cycles and WDT & LVDT are disabled

Sym	Description	Conditions	Min.	Typ.	Max.	Unit
F_{HF}	X'tal oscillation range	HF mode, Vdd=5V	1		20	MHz
		HF mode, Vdd=3V	1		15	
F_{XT}	X'tal oscillation range	XT mode, Vdd=5V	0.5		10	MHz
		XT mode, Vdd=3V	0.5		10	
F_{LF}	X'tal oscillation range	LF mode, Vdd=5V	32		4000	KHZ
		LF mode, Vdd=3V	32		1000	
F_{RC}	RC oscillation range	RC mode, Vdd=5V	DC		15	MHz
		RC mode, Vdd=3V	DC		7	
V_{IH}	Input high voltage	I/O ports, Vdd=5V	2.0			V
		RSTB, T0CKI pins, Vdd=5V	4.0			
		I/O ports, Vdd=3V	1.5			
		RSTB, T0CKI pins, Vdd=3V	2.4			
V_{IL}	Input low voltage	I/O ports, Vdd=5V			1.0	V
		RSTB, T0CKI pins, Vdd=5V			1.0	
		I/O ports, Vdd=3V			0.6	
		RSTB, T0CKI pins, Vdd=3V			0.6	
V_{OH}	Output high voltage	IOB0, IRSC=1, I_{OH}=-5.4mA, Vdd=5V	3.6			V
		IOB0, IRSC=0, I_{OH}=-5.4mA, Vdd=5V				
		Other pins, I_{OH}=-5.4mA, Vdd=5V				
V_{OL}	Output low voltage	IOB0, IRSC=1, I_{OL}=8.7mA, Vdd=5V			0.6	V
		IOB0, IRSC=0, I_{OL}=8.7mA, Vdd=5V				
		Other pins, I_{OL}=8.7mA, Vdd=5V			0.6	
I_{PH}	Pull-high current	Input pin at Vss, Vdd=5V		-45		uA
I_{WDT}	WDT current	Vdd=5V		6.8	9	uA
		Vdd=3V		1	3	
T_{WDT}	WDT period	Vdd=5V		16.2		mS
		Vdd=3V		20.4		
I_{LVDT}	LVDT current	Vdd=5V LVDT = 1.8V		4	4	uA
		Vdd=3V LVDT = 1.8V		2	3	
I_{SB}	Power down current	Sleep mode, Vdd=5V, WDT enable		9.8		uA
		Sleep mode, Vdd=5V, WDT disable		3		
		Sleep mode, Vdd=3V, WDT enable		2.1		
		Sleep mode, Vdd=3V, WDT disable		1.1		
I_{DD}	Operating current	HF mode, Vdd=5V, 4 clock instruction				mA
		20MHz		2.04		
		15MHz		1.68		
		10MHz		1.28		
		4MHz		0.78		
		2MHz		0.62		

I_{DD}	Operating current	HF mode, Vdd=3V, 4 clock instruction				mA
		20MHz		0.92		
		15MHz		0.72		
		10MHz		0.54		
		4MHz		0.30		
		2MHz		0.19		
I_{DD}	Operating current	HF mode, Vdd=5V, 2 clock instruction				mA
		20MHz		2.94		
		15MHz		2.34		
		10MHz		1.74		
		4MHz		0.96		
		2MHz		0.68		
I_{DD}	Operating current	HF mode, Vdd=3V, 2 clock instruction				mA
		20MHz		1.38		
		15MHz		1.07		
		10MHz		0.77		
		4MHz		0.38		
		2MHz		0.24		
I_{DD}	Operating current	XT mode, Vdd=5V, 4 clock instruction				mA
		20MHz		1.69		
		15MHz		1.36		
		10MHz		1.04		
		4MHz		0.64		
		2MHz		0.49		
I_{DD}	Operating current	XT mode, Vdd=3V, 4 clock instruction				mA
		20MHz		0.78		
		15MHz		0.60		
		10MHz		0.44		
		4MHz		0.24		
		2MHz		0.17		
I_{DD}	Operating current	XT mode, Vdd=5V, 2 clock instruction				mA
		20MHz		2.81		
		15MHz		2.20		
		10MHz		1.60		
		4MHz		0.87		
		2MHz		0.61		
I_{DD}	Operating current	XT mode, Vdd=3V, 2 clock instruction				mA
		20MHz		1.36		
		15MHz		1.05		
		10MHz		0.73		
		4MHz		0.36		
		2MHz		0.23		

I_{DD}	Operating current	LF mode, Vdd=5V, 4 clock instruction						uA
		2MHz				290		
		1MHz				208		
		500KHz				167		
		100KHz				118		
		32KHz				101		
I_{DD}	Operating current	LF mode, Vdd=3V, 4 clock instruction						uA
		2MHz				105		
		1MHz				73		
		500KHz				54		
		100KHz				33		
		32KHz				26		
I_{DD}	Operating current	LF mode, Vdd=5V, 2 clock instruction						uA
		2MHz				371		
		1MHz				269		
		500KHz				194		
		100KHz				130		
		32KHz				108		
I_{DD}	Operating current	LF mode, Vdd=3V, 2 clock instruction						uA
		2MHz				158		
		1MHz				100		
		500KHz				67		
		100KHz				38		
		32KHz				29		
I_{DD}	Operating current	RC mode, Vdd=5V, 4 clock instruction						mA
		C=3P	R=1Kohm	F=14.96MHz		4.572		
			R=3.3Kohm	F=11.06MHz		1.845		
			R=10Kohm	F=5.80MHz		0.761		
			R=100Kohm	F=808KHz		0.170		
			R=300Kohm	F=276KHz		0.119		
		C=20P	R=1Kohm	F=11.7MHz		4.226		
			R=3.3Kohm	F=6.35MHz		1.519		
			R=10Kohm	F=2.73MHz		0.613		
			R=100Kohm	F=320KHz		0.147		
			R=300Kohm	F=108KHz		0.109		
		C=100P	R=1Kohm	F=5.23MHz		3.429		
			R=3.3Kohm	F=2.05MHz		1.163		
			R=10Kohm	F=748KHz		0.454		
			R=100Kohm	F=80KHz		0.126		
			R=300Kohm	F=26.4KHz		0.100		
		C=300P	R=1Kohm	F=2.5MHz		3.024		

			R=3.3Kohm	F=900KHz		1.021		
			R=10Kohm	F=316KHz		0.403		
			R=100Kohm	F=32KHz		0.119		
			R=300Kohm	F=10.67KHz		0.098		
		RC mode, Vdd=3V, 4 clock instruction						
		C=3P	R=1Kohm	F=8.29MHz		2.280		
			R=3.3Kohm	F=7.2MHz		0.913		
			R=10Kohm	F=4.58MHz		0.396		
			R=100Kohm	F=900KHz		0.071		
			R=300Kohm	F=316KHz		0.040		
		C=20P	R=1Kohm	F=7MHz		2.214		
			R=3.3Kohm	F=5.1MHz		0.837		
			R=10Kohm	F=2.71MHz		0.327		
			R=100Kohm	F=374KHz		0.058		
I_{DD}	Operating current		R=300Kohm	F=128KHz		0.035		mA
		C=100P	R=1Kohm	F=4.14MHz		2.060		
			R=3.3Kohm	F=2.11MHz		0.688		
			R=10Kohm	F=848KHz		0.253		
			R=100Kohm	F=96KHz		0.047		
			R=300Kohm	F=32KHz		0.030		
		C=300P	R=1Kohm	F=2.36MHz		1.890		
			R=3.3Kohm	F=972KHz		0.630		
			R=10Kohm	F=360KHz		0.226		
			R=100Kohm	F=38KHz		0.043		
			R=300Kohm	F=12.71KHz		0.028		
		RC mode, Vdd=5V, 2 clock instruction						
		C=3P	R=1Kohm	F=15.16MHz		5.435		
			R=3.3Kohm	F=11.27MHz		2.358		
			R=10Kohm	F=5.77MHz		986		
			R=100Kohm	F=826KHz		0.183		
			R=300Kohm	F=274KHz		0.108		
		C=20P	R=1Kohm	F=11.56MHz		4.835		
			R=3.3Kohm	F=6.12MHz		1.808		
			R=10Kohm	F=2.72MHz		0.701		
			R=100Kohm	F=308KHz		0.138		
I_{DD}	Operating current		R=300Kohm	F=105KHz		0.092		mA
		C=100P	R=1Kohm	F=5.32MHz		3.680		
			R=3.3Kohm	F=1.99MHz		1.234		
			R=10Kohm	F=722KHz		0.479		
			R=100Kohm	F=77KHz		0.110		
			R=300Kohm	F=25.0KHz		0.081		
		C=300P	R=1Kohm	F=2.52MHz		3.107		
			R=3.3Kohm	F=892KHz		1.057		
			R=10Kohm	F=312KHz		0.398		
			R=100Kohm	F=32KHz		0.102		
			R=300Kohm	F=11KHz		0.077		

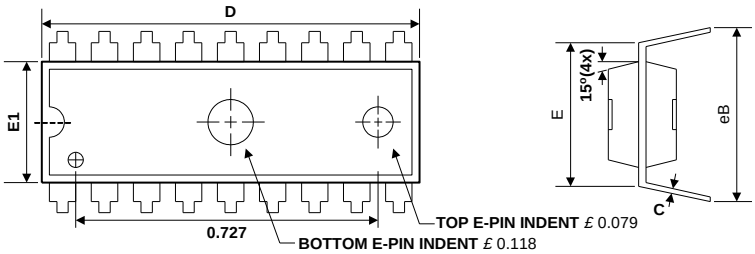
I_{DD}	Operating current	RC mode, Vdd=3V, 2 clock instruction						mA
		C=3P	R=1Kohm	F=8.306MHz		2.552		
			R=3.3Kohm	F=7.29MHz		1.130		
			R=10Kohm	F=4.81MHz		0.518		
			R=100Kohm	F=904KHz		0.084		
			R=300Kohm	F=338KHz		0.039		
		C=20P	R=1Kohm	F=7.08MHz		2.445		
			R=3.3Kohm	F=5.07MHz		0.986		
			R=10Kohm	F=2.68MHz		0.393		
			R=100Kohm	F=362KHz		0.061		
			R=300Kohm	F=123KHz		0.031		
		C=100P	R=1Kohm	F=4.11MHz		2.197		
			R=3.3Kohm	F=2.03MHz		0.745		
			R=10Kohm	F=810KHz		0.270		
			R=100Kohm	F=91KHz		0.043		
			R=300Kohm	F=30KHz		0.025		
		C=300P	R=1Kohm	F=2.37MHz		1.953		
			R=3.3Kohm	F=964KHz		0.648		
			R=10Kohm	F=354KHz		0.231		
			R=100Kohm	F=38KHz		0.038		
			R=300Kohm	F=13KHz		0.022		

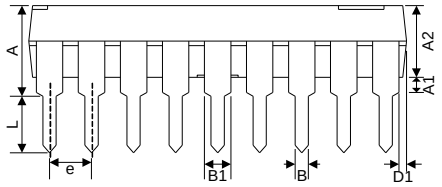
6.2 ELECTRICAL CHARACTERISTICS of AT8A22

To be defined

7.0 PACKAGE DIMENSION

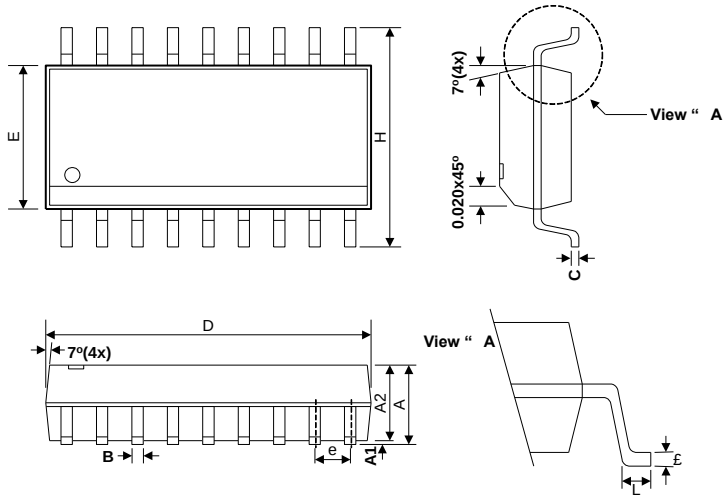
7.1 18-PIN PDIP 300mil





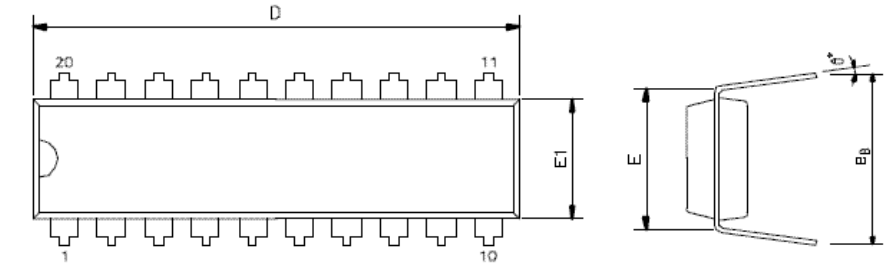
Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	-	-	4.57	-	-	0.180
A1	0.13	-	-	0.005	-	-
A2	-	3.30	3.56	-	0.130	0.140
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.33	0.008	0.010	0.013
D	22.71	22.96	23.11	0.894	0.904	0.910
D1	0.43	0.56	0.69	0.017	0.022	0.027
E	7.62	-	8.26	0.300	-	0.325
E1	6.40	6.50	6.65	0.252	0.256	0.262
e	-	2.54	-	-	0.100	-
L	3.18	-	-	0.125	-	-

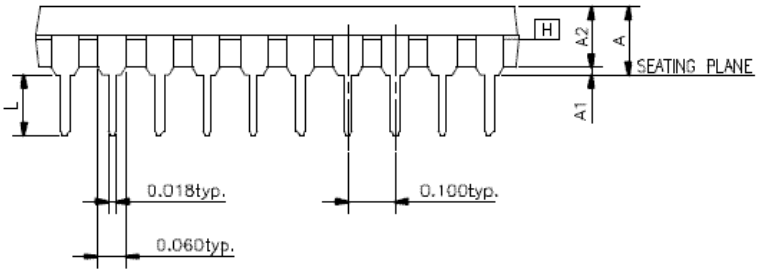
7.2 18-PIN SOP 300mil



Symbols	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.36	2.49	2.64	0.093	0.098	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	-	2.31	-	-	0.091	-
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.18	0.23	0.28	0.007	0.009	0.011
D	11.35	-	11.76	0.447	-	0.463
E	7.39	7.49	7.59	0.291	0.295	0.299
e	-	1.27	-	-	0.050	-
H	10.01	10.31	10.64	0.394	0.406	0.419
L	0.38	0.81	1.27	0.015	0.032	0.050
θ	0°	-	8°	0°	-	8°

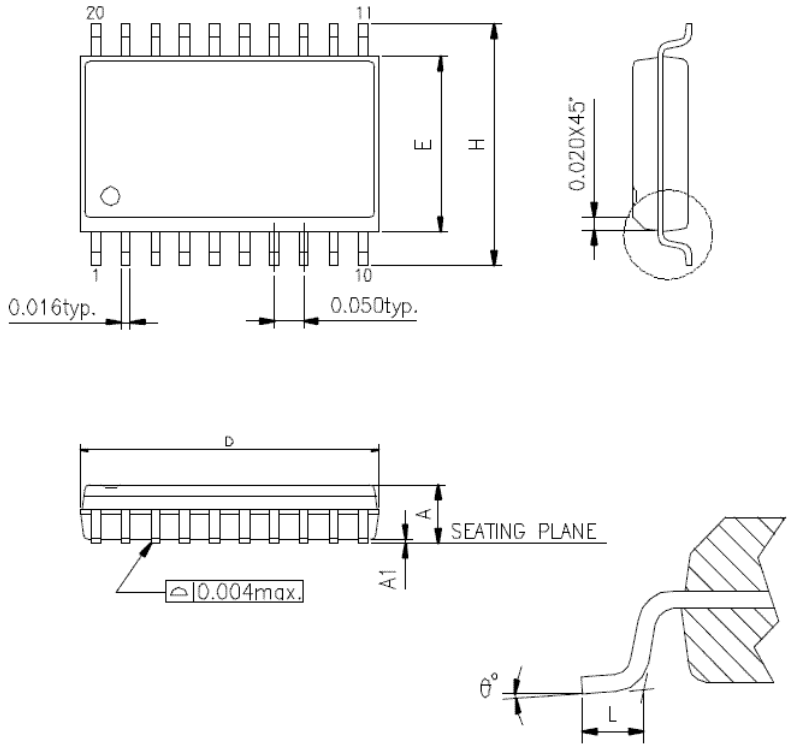
7.3 20-PIN PDIP





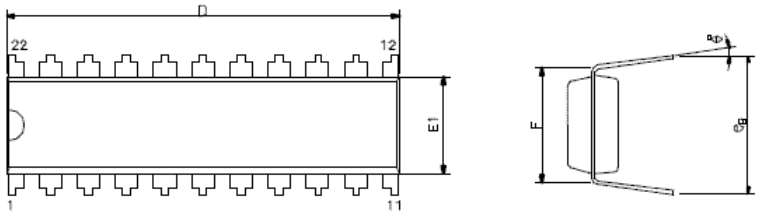
Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	0.98	1.030	1.060
E		0.300 BSC	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

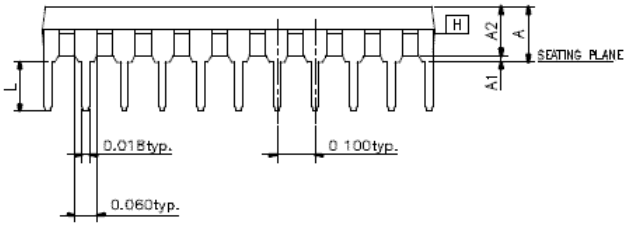
7.4 20-PIN SOP



Symbols	Dimension In Inches		
	Min	Nom	Max
A	0.093	-	0.104
A1	0.004	-	0.012
D	0.496	-	0.508
E	0.291	-	0.299
H	0.394	-	0.419
L	0.016	-	0.050
θ°	0°	-	8°

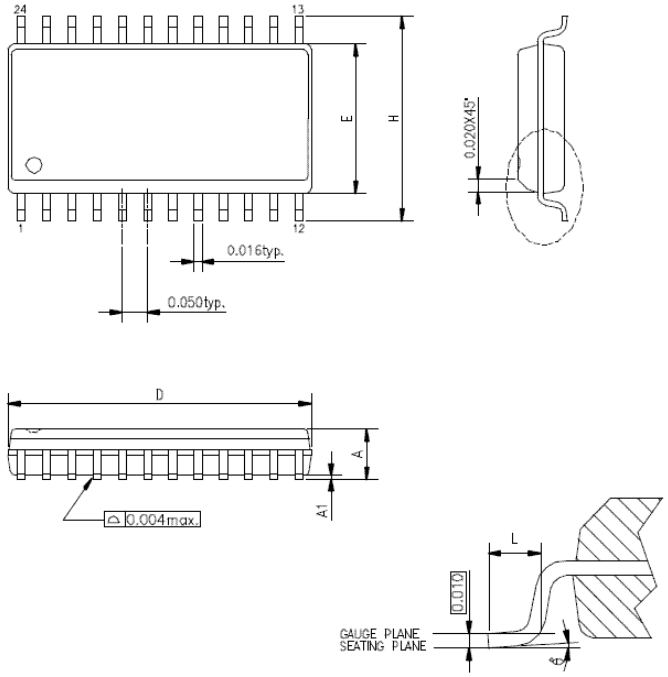
7.5 22-PIN SKINNY PDIP





Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.210
A1	0.015	-	-
A2	0.125	0.130	0.135
D	1.020	1.030	1.060
E	0.300 BSC		
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
eB	0.335	0.355	0.375
θ°	0°	7°	15°

7.6 24-PIN SOP



Symbols	Dimension In Inches		
	Min	Nom	Max
A	-	-	0.104
A1	0.004	-	-
D	0.599	0.600	0.624
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0°	4°	8°

8.0 ORDERING INFORMATION

OTP Type MCU	Package Type	Pin Count	Package Size
AT8A22AEP	PDIP	18	300 mil
AT8A22AED	SOP	18	300 mil
AT8A22BEP	PDIP	20	300 mil
AT8A22BED	SOP	20	300 mil
AT8A22CEM	Skinny PDIP	22	300 mil
AT8A22DED	SOP	24	300 mil

Mask Type MCU	Package Type	Pin Count	Package Size
AT8A22AP	PDIP	18	300 mil
AT8A22AD	SOP	18	300 mil
AT8A22BP	PDIP	20	300 mil
AT8A22BD	SOP	20	300 mil
AT8A22CM	Skinny PDIP	22	300 mil
AT8A22DD	SOP	24	300 mil